Chapter 2
Previous Works on Automated Analog IC Sizing

Abstract In the last 25 years, the scientific community proposed many techniques for the automation of analog integrated circuit sizing. In this chapter, those approaches are briefly surveyed, focusing on the optimization techniques that are used. The different approaches are classified in terms of the techniques used and the most significant aspects observed were the setup and the execution time, as well as the accuracy in the evaluation of the solutions. The study is then used to select the optimization methods to be considered in the developed framework.

2.1 Automatic IC Sizing

Analog IC sizing automation techniques are classified into two main groups, the knowledge-based approaches and the optimization-based approaches [1]. This classification is based on the fundamental techniques used to address the problem, as illustrated in Fig. 2.1.

2.1.1 Knowledge-Based Automatic Circuit Sizing

Early automation systems [2–5] did not use optimization and tried to systematize the design by using a design plan derived from expert knowledge. In these methods, a plan is built with design equations and a design strategy that produces the component sizes that meet the performance requirements. These knowledge-based approaches were applied with moderate success. The main advantage of this approach is the short execution time. However, deriving the design plan is hard and time-consuming, and the design plan requires constant maintenance in order to keep
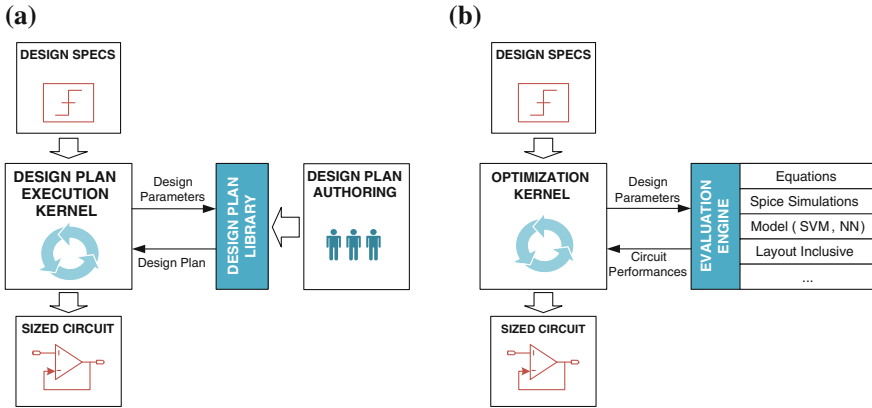
(a)   **(b)**

Fig. 2.1 Automatic circuit sizing approaches; **a** knowledge-based; **b** optimization-based

it up to date with technological evolution, also, the results are not optimal, suitable only as a first-cut-design.

The next generations of sizing tools apply optimization techniques to analog IC sizing. They can be further classified into two main subclasses: equation-based or simulation-based, from the method used to evaluate the circuit's performance.

2.1.2 Equation-Based Automatic Circuit Sizing

Equation-based methods use analytic expressions to relate the circuit's performance figures to the design variables. Different optimization techniques are used, both deterministic and stochastic. Knowing the equations and their properties allows the use of classical optimization methods. In OPASYN [6], the optimization is performed using steepest descent; similarly, in STAIC [7], it is used as a successive solution refinements technique.

Maulik et al. [8, 9] define the sizing problem as a constrained nonlinear optimization problem using spice models and DC operating point constraints, solving it using sequential quadratic programming. Matsukawa et al. [10] design $\Delta\Sigma$ and pipeline analog to digital converters solving, via convex optimization the equations that relate the performance of the converter to the size of the components.

In GPCAD [11], a posynomial circuit model is optimized using Geometrical Programming (GP); the execution time is in the order of few seconds, but the general application of posynomial models is difficult and the time to derive the model for new circuits is still high. Kuo-Hsuan et al. [12] revisited the posynomial modeling recently, surpassing the accuracy issue by introducing an additional generation step, where local optimization using simulated annealing (SA) and a circuit simulator is performed. The same strategy is applied in FASY [13, 14], where analytical

expressions are solved to generate an initial solution and a simulation-based optimization is performed to fine tune the solution.

Other equation-based approaches do not limit the problem formulation in order to use a specific optimization technique at all, relying on heuristic optimization instead. OPTIMAN [15] uses SA applied to analytical models, and, in ASTRX/ OBLX [16], an SA optimization is also performed using cost function defined by equations for dc operation point, and small signal Asymptotic Waveform Evaluation (AWE)-based simulation; this evaluation technique is also used in DARWIN [17], which uses Genetic Algorithms (GA) instead. Doboli et al. [18] also apply genetic programming techniques to simultaneously derive the sub-block specifications, sub-block topology selection, and transistor sizing.

Equation-based methods' strong point is the short evaluation time, making them, like the knowledge-based approaches, extremely suited to derive first-cut designs. The main drawback is that, despite the advances in symbolic analysis, not all design characteristics can be easily captured by analytic equations, making the generalization of the method to different circuits very difficult. In addition, the approximations introduced in the equations yield low accuracy designs, especially for complex circuits, requiring additional work to ensure that the circuit really meets the specifications.

2.1.3 Simulation-Based Automatic Circuit Sizing

With the availability of computing resources, simulation-based optimization gained ground, and is the most common method found in recent approaches. In simulation-based sizing, as in the case of AIDA-C, a circuit simulator, e.g., SPICE [19], is used to evaluate the circuit performance.

Early approaches to simulation-based automatic sizing used local optimization around a "good" solution, where SA [20] is the most commonly optimization technique used. In DELIGTH.SPICE [21], the optimization algorithm (phase I-II-III method of feasible directions) is used to perform local design optimization around a user provided starting point. Kuo-Hsuan et al. [12] and FASY [13, 14] use equation-based techniques to derive an approximate solution, and then use simulation within a SA kernel to optimize the design. Likewise, Cheng et al. [22] also uses SA but considers the transistor bias conditions to constrain the problem, and, instead of solving the circuit by finding transistor sizes, the problem is solved by finding the bias of the transistors. FRIDGE [23] aims for general applicability approach by using an annealing-like optimization without any restriction to the starting point. Castro-Lopez et al. [24] use SA followed by a deterministic method for fine-tuning to perform the optimization.

Another widely used class of optimization methods is the GA. Barros et al. in [1, 25, 26] presents a circuit sizing optimization supported by a genetic algorithm where the evaluations of the populations were made using both a circuit simulator and an automatically trained support vector machine. Alpaydin et al. [27] use

hybridization of evolutionary and annealing optimization strategy where the circuits' performance figures are computed using a blend of equations and simulations.

Given the affinity evolutionary algorithms have with parallel implementations, in Santos-Tavares [28], MAELSTROM [29], and ANACONDA [30] the time to simulate the population reduced by a parallel mechanism that shares the evaluation load among multiple computers. Because the traditional use of local search methods in many implementations, the MAELSTROM's authors option was to use a hybridization, i.e., the parallel recombinative simulated annealing (PRSA). In ANACONDA the approach is similar but instead of the PRSA it is applied a variation of pattern search algorithms, named by the authors as stochastic pattern search.

A different approach to circuit sizing optimization that also employs evolutionary methods is to simultaneously generate the circuit topologies (the arrangement of the devices) and the device sizes. Koza [31], Sripramong [32], and more recently Hongying [33] proposed a design methodology able to create new topologies by exploring the immense possibilities starting from low abstraction level. Small elementary blocks are connected bottom-up to each other to form a new topology. Various fundamental entities can be applied, such as, single transistors, elementary building blocks, or node connections. However, these approaches are met with great skepticism, as designers are suspicious of the generated structures, because they often differ "too" much from the well-known analog circuit structures.

Swarm intelligence algorithms [34] can also be found in the literature applied to analog circuit sizing. The fundament of swarm intelligence algorithms is to use many simple agents that lead an intelligent global behavior, like the one observed in many insect hives. From these methods, the most commons are the ant colony optimization (ACO), which was successfully applied in [35, 36], and particle swarm optimization (PSO) that can be found in [37–39].

Circuit sizing is in its essence a multi-objective multi-constraint problem, and the designer often explores the tradeoff among contradictory performance measures, for example, minimizing power consumption while maximizing bandwidth, or maximizing gain and minimizing area of an amplifier, as such, the usage of multi-objective optimization techniques is becoming more common. When considering multiple objectives the output is not one solution, but a set of optimal design tradeoff solutions, usually referred as Pareto optimal front (POF). Given the multiple elements already present in both evolutionary and swarm intelligence algorithms, these are the natural candidates to implement such approach. In GENOM-POF [40, 41] and MOJITO [42], the evolutionary multi-objective methods are applied, respectively, to circuit sizing and both sizing and topology exploration, whereas in [39] particle swarm optimization is explored in both single and multi-objective approaches. A different approach is taken by Pradhan and Vemuri in [43], where the multi-objective simulated annealing (MOSA) is used.

Instead of executing circuit sizing on-the-fly, in some approaches, the non-dominated solutions are generated, prior to the design task, using the previously referred multi-objective optimization methods or variations of them for the most

relevant tradeoff and then, the suitable solution is selected from the already sized solutions [44–47].

From the study of analog circuit sizing and optimization approaches proposed by the scientific community recently, it is clear that there is not a specific trend toward a single algorithm, but many were experimented with. In the next section, the summary of the surveyed approaches is presented, and finally the objectives for this work are refined, namely the selection of the optimization kernels to be initially included in the platform.

2.2 Optimization Techniques Applied to Analog Circuit Sizing

The analog sizing tools approaches surveyed are summarized in Table 2.1. In the equation-based systems, the usage of classical optimization methods is possible; however, the accuracy of the models and the derivation of such equations strongly limit the applicability. This limitation of the equation-based systems is overcome at the expense of evaluation time by using accurate circuit simulation to evaluate the performance figures being optimized.

Using the circuit simulator, methods that take advantage of some properties of the models that cannot be used, leading, as seen, to the usage of stochastic heuristic optimization techniques. From the approaches that were surveyed, the most common stochastic algorithms were based on simulation annealing and genetic/evolutionary approaches, with some of the latest implementations considering particle swarm optimization and ant colony methods.

2.2.1 Selection of Optimization Methods

This work is in the scope of circuit sizing which considers electric simulation to evaluate the circuits' performance, as illustrated in Fig. 2.2. The generality of the approach is increased and the setup time for new circuits is decreased. However, the relation between the performance figures and the design variables becomes unknown, making the usage of classic optimization methods inappropriate, as seen in the surveyed simulation-based systems where almost all consider heuristic optimization methods.

In AIDA-C, the circuit sizing and optimization problem, which will be described in detail in Chap. 3, is modeled as a multi-objective multi-constraint optimization problem. In this context, special relevance is given to multi-objective algorithms. Historically, both SA and GA have been used intensively, in this sense, it is natural to consider at least an evolutionary and an annealing. Given the recent experiments

Table 2.1 Summary of analog IC design automation tools for sizing and optimization

Tool/author		Design plan/ optimization method	Evaluation	Time setup/ exec.
IDAC [4]	1987	Design plan plus SA post-optimization	Equations	Months/few seconds
DELIGTH.SPICE [21]	1988	Feasible directions optimization	Simulator	Moderate/18 h
OPASYN [6]	1990	Steepest descent	Equations	2 weeks/5 min
OPTIMAN [15]	1990	SA	Equations	◊/1 min
STAIC [7]	1992	two-step optimization	Equations	Long/2 min
Maulik et al. [8, 9]	1993	B&B, and sequential quadratic program	Equations and BSIM models	6 months/1 min
FRIDGE [23]	1994	SA	Simulator	1 h/45 min
DARWIN [17]	1995	GA	Small signal, analytical expressions	◊/◊
ISAID [2, 3]	1995	Qualitative reasoning + post optimization	Equations and qualitative reasoning	◊/◊
FASY [13, 14]	1996	SA + Gradient	Simulator	◊/6 h
ASTRX/OBLX [16]	1996	SA	AWE equations	Few days/few seconds
Koza [31]	1997	GA	Simulator	◊/◊
GPCAD [11]	1998	Geometric programming	Posynomial	◊/fast
MAELSTROM [29]	1999	GA + SA	Simulator	◊/3, 6 h
ANACONDA [30]	2000	Stochastic pattern search	Simulator	◊/10 h
Sripramong [32]	2002	GA	Simulator	◊/3 days
Alpaydin [27]	2003	Evolutionary strategies + SA	Fuzzy + NN trained with Simulator	◊/45 min
Shoou-Jin [48]	2006	GA	Equations	◊/◊
Barros [1, 25, 26]	2006	GA	Simulator	◊/20 min
Castro-Lopez [24]	2008	SA + Powell's method	Simulator	◊/25 min
Santos-Tavares [28]	2008	GA	Simulator	◊/◊
MOJITO [42]	2009	NSGA-II	Simulator	◊/<7 days
Pradhan [43]	2009	Multi-objective SA	Layout aware MNA models	◊/16 min
Matsukawa [10]	2009	Convex optimization	Convex functions	◊/◊
Cheng [22]	2009	SA	Equations	◊/<1 h
Hongying [33]	2010	GA with VDE	Simulator	◊/◊
Fakhfakh [39]	2010	Multi-objective PSO	Equations	◊/<1 min

(continued)

Table 2.1 (continued)

| Tool/author		Design plan/ optimization method	Evaluation	Time setup/ exec.
Kuo-Hsuan [12]	2011	Convex optimization	Posynomial	⊘/1 h
		Stochastic fine tuning	Simulator	
Kamisetty et al. [37]	2011	PSO		⊘/⊘
Benhala et al. [36]	2012	ACO	Equation	⊘/<1 min
Roca et al. [46]	2012	NSGA-II	Simulator	⊘/⊘
Gupta and Gosh [35]	2012	ACO	Simulator	⊘/<2 h
Kumar and Duraiswamy [38]	2012	PSO	Simulator	⊘/⊘
Genom-POF [40, 41]	2012	NSGA-II	Simulator	⊘/<1 h
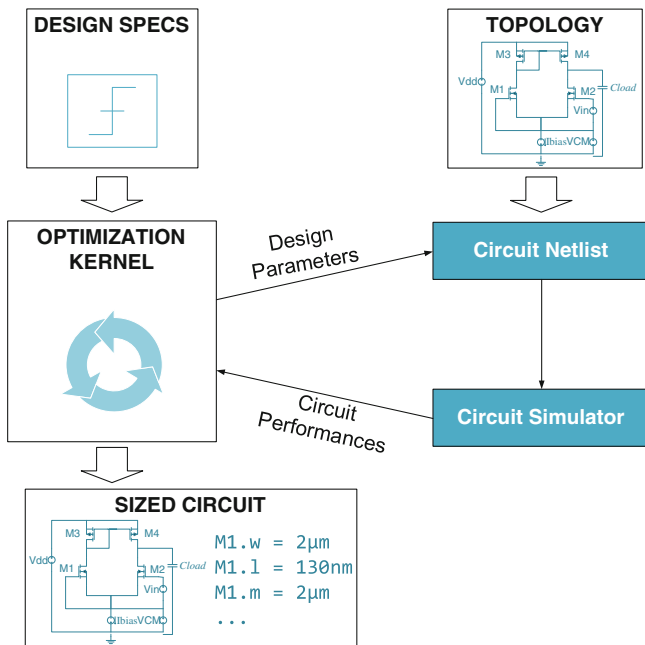
Fig. 2.2 Automatic optimization-based circuit sizing using simulator

with swarm intelligence in this domain, and to broad the scope of the implemented framework, this class of methods should also be considered.

From a brief perusal of the multi-objectives implementations, the ideas like non-sorted domination or crowding distance (further described in Chap. 3) presented in NSGA-II are reused by several other methods, as that the advantages of the inclusion of NSGAII in the framework are clear. Given the usage of SA, some sort

of multi-objective SA should also be considered. In terms of the swarm intelligence algorithms, both ACO and PSO have been applied to circuit sizing. Because MOPSO is already found in the literature and the unnatural application to real valued problems of the path finding ideas of the ACO, MOPSO will be considered.

2.3 Conclusions

In this survey, several ADA tools were presented and analyzed to better understand the advantages, and drawbacks, that can be improved in the future. It was also possible to identify that a wide range of optimization techniques are considered in this domain and new ones are always being introduced.

In this work, AIDA-CMK improves AIDA-C by adding a flexible and systematic manner to try and experiment new optimization techniques, so that further improvements to the automation of analog circuits design, namely in the circuit sizing and optimization, can be implemented more efficiently. The trends in optimization methods were also surveyed, showing a predominance of the multi-objective approaches in recent works, and the presented study was used to select a set of methods that will be considered initially to demonstrate the proposed solution.

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