Preface

CMOS spiral inductors have found a broad range of applications in high-speed analog signal processing and data communications. These applications include bandwidth enhancement, delay reduction, impedance matching, frequency selection, distributed amplifiers, RF phase shifters, low-noise amplifiers, and voltage-controlled oscillators, to name a few. The effectiveness of these inductors, however, is affected by a number of limitations intrinsic to the spiral layout of the inductors. These limitations include a low quality factor, a low self-resonant frequency, a small and non-tunable inductance, and the need for a prohibitively large silicon area. The use of CMOS spiral transformers in RF applications such as low-noise amplifiers, power amplifiers, and LC oscillators has emerged recently. These transformers are constructed by coupling two spiral inductors via a magnetic link. They offer the advantages of a reduced silicon consumption and increased inductances. The limitations of spiral inductors, however, are inherited by spiral transformers.

Inductors and transformers synthesized using active devices, known as active inductors and transformers, offer a number of unique advantages over their spiral counterparts including virtually no chip area requirement, large and tunable inductances with large inductance tuning ranges, large and tunable quality factors, high self-resonant frequencies, and full compatibility with digital oriented CMOS technologies. Active inductors and transformers have found increasing applications in high-speed analog signal processing and data communications where spiral inductors and transformers are usually employed. As compared with spiral inductors and transformers, the applications of CMOS active inductors and transformers are affected by a number of limitations intrinsic to synthesized devices. These limitations include a small dynamic range, poor noise performance, a high level of power consumption, and a high sensitivity to supply voltage fluctuation and process variation.

This book provides a comprehensive treatment of the principle, topologies, and characteristics of CMOS active inductors and transformers, and an in-depth

examination of their emerging applications in high-speed analog signal processing and data communications. The materials presented in the book are based on the work of many researchers who contributed to the theory and design of CMOS active inductors and transformers. In recognition of their contributions, the active inductors and transformers presented in this text are named in the names of the researchers. For active inductors and transformers developed by more than two researchers, although due to the space constraint, only the name of the first author of the work is used to name the active inductors and transformers, the contributions of all other authors are equally recognized. This is reflected by the presentation of the full authorship of the work in the *References* of the book. The same approach is followed in the presentation of CMOS active inductor/transformer bandpass filters, oscillators, and other sub-systems.

This book consists of two parts : Part I - *Principle and Implementation of CMOS Active Inductors and Transformers*, and Part II -*Applications of CMOS Active Inductors and Transformers*.

Part I of the book deals with the topologies, characteristics and implementation of CMOS active inductors and transformers. This part consists of three chapters.

Chapter 1 starts with a brief investigation into why inductive characteristics are critically needed in high-speed applications. This is demonstrated with the applications of inductors and transformers in LC oscillators, impedance matching networks, RF phase shifters, RF power dividers, frequency selection networks, in particular, RF bandpass filters, and low-noise amplifiers. A detailed examination of the design constraints of monolithic inductors and transformers is followed. The advantages and design challenges of CMOS active inductors and transformers are examined in detail.

Chapter 2 presents the principles of the synthesis of inductors using gyrator-C networks. Both lossless and lossy single-ended and fully differential gyrator-C active inductors are studied. The important figure-of-merits that quantify the performance of active inductors including frequency operation range, inductance tunability, quality factor, noise, linearity, stability, supply voltage sensitivity, parameter sensitivity, signal sensitivity, and power consumption are examined in detailed. The details of the CMOS implementation and analysis of single-ended and fully differential active inductors are presented. The circuit implementation and characteristics of published CMOS active inductors are examined in detail.

Chapter 3 focuses on the principles of the synthesis of CMOS active transformers. Both lossless and lossy gyrator-C active transformers are studied. The characterization of active transformers including stability, frequency operation range, the tunability of self and mutual inductances, turn ratios, coupling

factors, voltage and current transfer characteristics, impedance transformation, noise, quality factors, linearity, supply voltage sensitivity, parameter sensitivity, and power consumption is examined in detail. The CMOS implementation of several published CMOS active transformers is presented and their characteristics are analyzed.

Part II of the book focuses upon the emerging applications of CMOS active inductors and transformers in high-speed analog signal processing and data communications. This part consists of four chapters.

Chapter 4 investigates the implementation and characteristics of RF bandpass filters using CMOS active inductors. The chapter starts with a detailed investigation of the characterization of bandpass filters. Bandwidth, 1-dB compression points, third-order intercept points, noise figure, noise bandwidth, spurious-free-dynamic range, frequency selectivity, and passband center frequency tuning are examined. It is followed by a detailed examination of the configurations of RF bandpass filters with active inductors. Wu bandpass filters, Thanachayanont bandpass filters, Xiao-Schaumann bandpass filters, Thanachayanont-Payne bandpass filter, and Weng-Kuo bandpass filters are studied and their performance is compared.

Chapter 5 looks into the realization of the building blocks of high-speed transceivers using CMOS active inductors and transformers. The use of CMOS active inductors in low-noise amplifiers, optical front-ends, RF phase shifters, RF modulators, RF power dividers, and Gb/s serial-link transceivers is examined in detail.

Chapter 6 starts with a brief review of the fundamentals of electrical oscillators. Both ring and LC oscillators are investigated. The use of CMOS active inductors in improving the performance of ring oscillators is investigated. The presentation continues with a close examination of the use of CMOS active inductors in LC oscillators. A special attention is given to the comparison of the phase noise of these oscillators. LC oscillators and LC quadrature oscillators using CMOS active transformers are also studied.

Chapter 7 presents the theory of current-mode phase-locked loops (PLLs) and examines the intrinsic differences between voltage-mode and current-mode PLLs. The chapter starts with an in-depth study of the configurations and characteristics of voltage-mode PLLs. Both type I and type II voltage-mode PLLs are studied. It then moves on to investigate current-mode PLLs with CMOS active inductors and transformers. The loop dynamics of these PLLs are investigated in detailed. Three design examples are utilized to demonstrate the performance of current-mode PLLs with active inductors and active transformers.

The materials of the book are presented with an emphasis on both the evolution of each class of circuits and a close comparison of their advantages and limitations. The examples given in the book were implemented in TSMC-

0.18μm 1.8V and UMC-0.13μm 1.2V CMOS technologies, and analyzed using SpectreRF from Cadence Design Systems with BSIM3v3RF device models that account for both the parasitics and high-order effects of MOS devices at high frequencies. Readers are assumed to be familiar with the fundamentals of electrical networks, microelectronic devices and circuits, signals and systems, and basic RF circuits.

This book is the first text that provides a comprehensive treatment of the principle, implementation, and applications of CMOS active inductors and transformers. It is a valuable resource for senior undergraduate / graduate students and an important reference for IC design engineers.

Although an immense amount of effort has been made in preparation of the manuscript, flaws and errors will still exist due to erring human nature. Suggestions and corrections will be gratefully appreciated by the author.

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Chapter 2

CMOS ACTIVE INDUCTORS

This chapter provides an in-depth treatment of the principles, topologies, characteristics, and implementation of CMOS active inductors. Section 2.1 investigates the principles of gyrator-C based synthesis of inductors. Both single-ended and floating (differential) configurations of gyrator-C active inductors are studied. Section 2.2 investigates the most important figure-of-merits that quantify the performance of active inductors. These figure-of-merits include frequency range, inductance tunability, quality factor, noise, linearity, stability, supply voltage sensitivity, parameter sensitivity, signal sensitivity, and power consumption. Section 2.3 details the CMOS implementation of single-ended gyrator-C active inductors. The schematics and characteristics of floating gyrator-C active inductors are examined in detail in Section 2.4. Class AB active inductors are investigated in Section 2.5. The chapter is summarized in Section 2.6.

2.1 Principles of Gyrator-C Active Inductors

2.1.1 Lossless Single-Ended Gyrator-C Active Inductors

A gyrator consists of two back-to-back connected transconductors. When one port of the gyrator is connected to a capacitor, as shown in Fig.2.1, the network is called the gyrator-C network. A gyrator-C network is said to be lossless when both the input and output impedances of the transconductors of the network are infinite and the transconductances of the transconductors are constant.

Consider the lossless gyrator-C network shown in Fig.2.1(a). The admittance looking into port 2 of the gyrator-C network is given by

$$Y = \frac{I_{in}}{V_2} = \frac{1}{s\left(\frac{C}{G_{m1}G_{m2}}\right)}. \tag{2.1}$$

Eq.(2.1) indicates that port 2 of the gyrator-C network behaves as a single-ended lossless inductor with its inductance given by

$$L = \frac{C}{G_{m1}G_{m2}}. \tag{2.2}$$

Gyrator-C networks can therefore be used to synthesize inductors. These synthesized inductors are called gyrator-C active inductors. The inductance of gyrator-C active inductor is directly proportional to the load capacitance C and inversely proportional to the product of the transconductances of the transconductors of the gyrator. Also, the gyrator-C network is inductive over the entire frequency spectrum. It should also be noted that the transconductor in the forward path can be configured with a negative transconductance while the transconductor in the feedback path has a positive transconductance, as shown in Fig.2.1(b).

Although the transconductors of gyrator-C networks can be configured in various ways, the constraint that the synthesized inductors should have a large frequency range, a low level of power consumption, and a small silicon area requires that these transconductors be configured as simple as possible. Fig.2.2 shows the simplified schematics of the basic transconductors that are widely used in the configuration of gyrator-C active inductors. Common-gate, common-drain, and differential-pair transconductors all have a positive transconductance while the common-source transconductor has a negative transconductance. To demonstrate this, consider the common-gate transconductor. An increase in v_{in} will lead to a decrease in i_D. Because $i_o = J - i_D$, i_o will increase accordingly. So the transconductance of the common-gate transconductor is positive. Similarly, for the differential-pair transconductor in Fig.2.2(d). An increase in v_{in} will result in an increase in i_{D1}. Since $i_{D2} = J_3 - i_{D1}$, i_{D2} will decrease. Further $i_o = J_2 - i_{D2}$, i_o will increase. The differential-pair transconductor thus has a positive transconductance.

2.1.2 Lossless Floating Gyrator-C Active Inductors

An inductor is said to be floating if both the terminals of the inductor are not connected to either the ground or power supply of the circuits containing the active inductor. Floating gyrator-C active inductors can be constructed in a similar way as single-ended gyrator-C active inductors by replacing single-ended transconductors with differentially-configured transconductors, as shown in Fig.2.3. Because

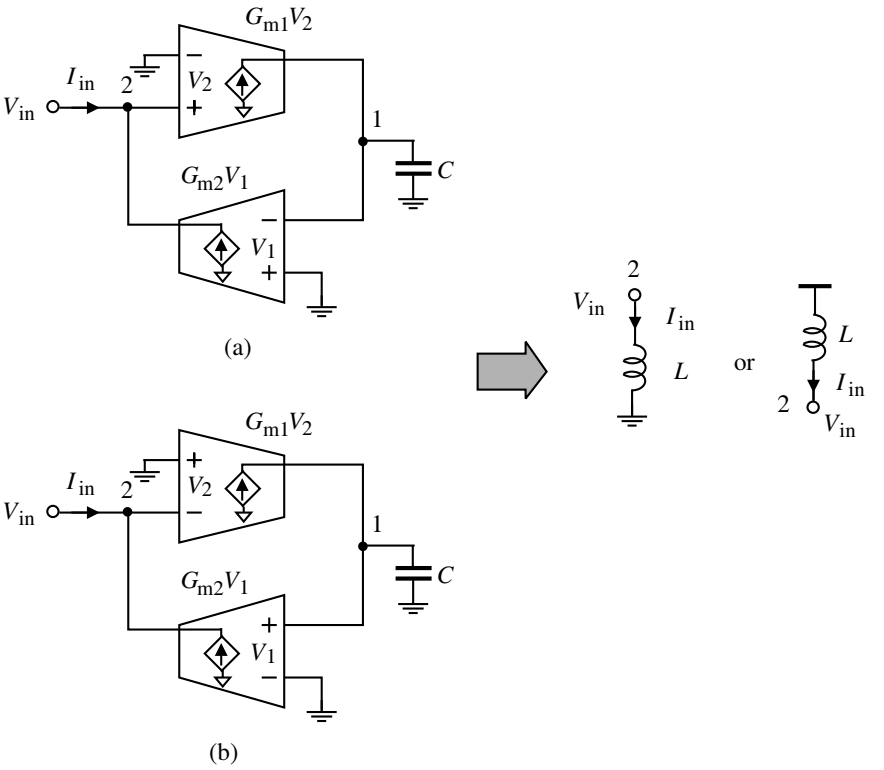


Figure 2.1. Lossless singe-ended gyrator-C active inductors. G_{m1} and G_{m2} are the transconductances of transconductors 1 and 2, respectively, and C is the load capacitance at node 1. (a) Transconductor in the forward path has a positive transconductance while the transconductor in the feedback path has a negative transconductance; (b) Transconductor in the forward path has a negative transconductance while the transconductor in the feedback path has a positive transconductance.

$$
\begin{aligned}
V_{in1}^{+} &= -\frac{g_{m1}}{sC}(V_{in2}^{+} - V_{in2}^{-}), \\
V_{in1}^{-} &= \frac{g_{m1}}{sC}(V_{in2}^{+} - V_{in2}^{-}), \\
I_{o2} &= g_{m2}(V_{in1}^{+} - V_{in1}^{-}),
\end{aligned}
\tag{2.3}
$$

we have

$$
I_{o2} = -\frac{2g_{m1}g_{m2}}{sC}(V_{in2}^{+} - V_{in2}^{-}). \tag{2.4}
$$

The admittance looking into port 2 of the gyrator-C network is given by

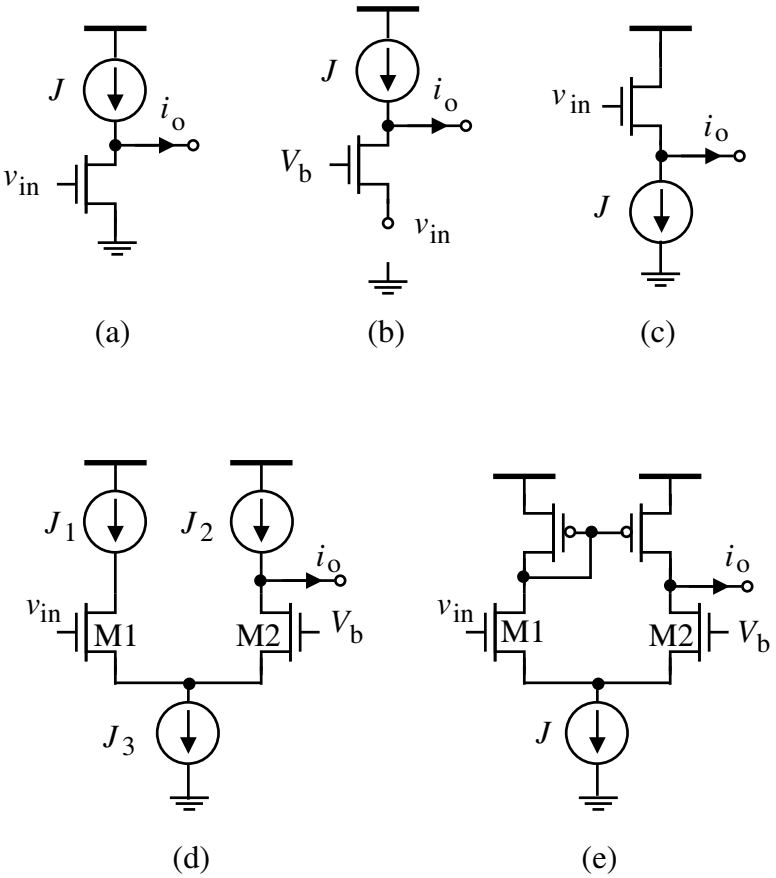


Figure 2.2. Simplified schematic of basic transconductors. (a) Common-source transconductor $i_o = -g_m v_{in}$; (b) Common-gate transconductor $i_o = g_m v_{in}$; (c) Common-drain (source follower) transconductor $i_o = g_m v_{in}$; (d,e) Differential-pair transconductors $i_o = g_m v_{in}$.

$$\begin{aligned} Y &= \frac{I_{in}}{V_{in2}^{+} - V_{in2}^{-}} \\ &= \frac{1}{s\left(\frac{2C}{g_{m1}g_{m2}}\right)}. \end{aligned} \tag{2.5}$$

Eq.(2.5) reveals port 2 of the gyrator-C network behaves as a floating inductor with its inductance given by

$$L = \frac{2C}{g_{m1}g_{m2}}. \tag{2.6}$$

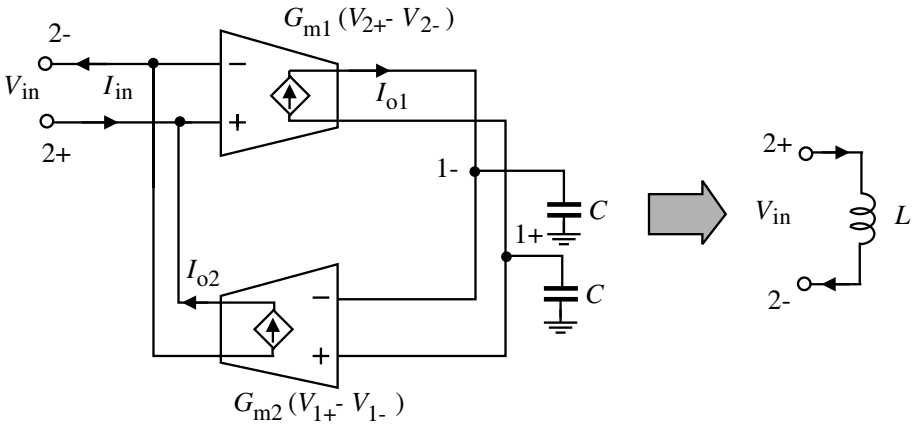


Figure 2.3. Lossless floating gyrator-C active inductors. G_{m1} and G_{m2} are the transconductances of transconductors 1 and 2, respectively, and C is the load capacitance at nodes 1+ and 1-.

Floating gyrator-C active inductors offer the following attractive advantages over their single-ended counterparts : (i) The differential configuration of the transconductors effectively rejects the common-mode disturbances of the network, making them particularly attractive for applications where both analog and digital circuits are fabricated on the same substrate. (ii) The level of the voltage swing of floating active inductors is twice that of the corresponding single-ended active inductors.

2.1.3 Lossy Single-Ended Gyrator-C Active Inductors

When either the input or the output impedances of the transconductors of gyrator-C networks are finite, the synthesized inductors are no longer lossless. Also, the gyrator-C networks are inductive only in a specific frequency range.

Consider the gyrator-C network shown in Fig.2.4 where G_{o1} and G_{o2} denote the total conductances at nodes 1 and 2, respectively. Note G_{o1} is due to the finite output impedance of transconductor 1 and the finite input impedance of transconductor 2. To simplify analysis, we continue to assume that the transconductances of the transconductors are constant. Write KCL at nodes 1 and 2

$$\begin{aligned} &(sC_1 + G_{o1})V_1 - G_{m1}V_2 = 0 \qquad \text{(node 1)}, \\ &-I_{in} + (sC_2 + G_{o2})V_2 - G_{m2}(-V_1) = 0, \quad \text{(node 2)}. \end{aligned} \tag{2.7}$$

The admittance looking into port 2 of the gyrator-C network is obtained from

$$\begin{aligned} Y &= \frac{I_{in}}{V_2} \\ &= sC_2 + G_{o2} + \frac{1}{s\Big(\frac{C_1}{G_{m1}G_{m2}}\Big) + \frac{G_{o1}}{G_{m1}G_{m2}}}. \end{aligned} \tag{2.8}$$

Eq.(2.8) can be represented by the RLC networks shown in Fig.2.4 with its parameters given by

$$\begin{aligned} R_p &= \frac{1}{G_{o2}}, \\ C_p &= C_2, \\ R_s &= \frac{G_{o1}}{G_{m1}G_{m2}}, \\ L &= \frac{C_1}{G_{m1}G_{m2}}. \end{aligned} \tag{2.9}$$

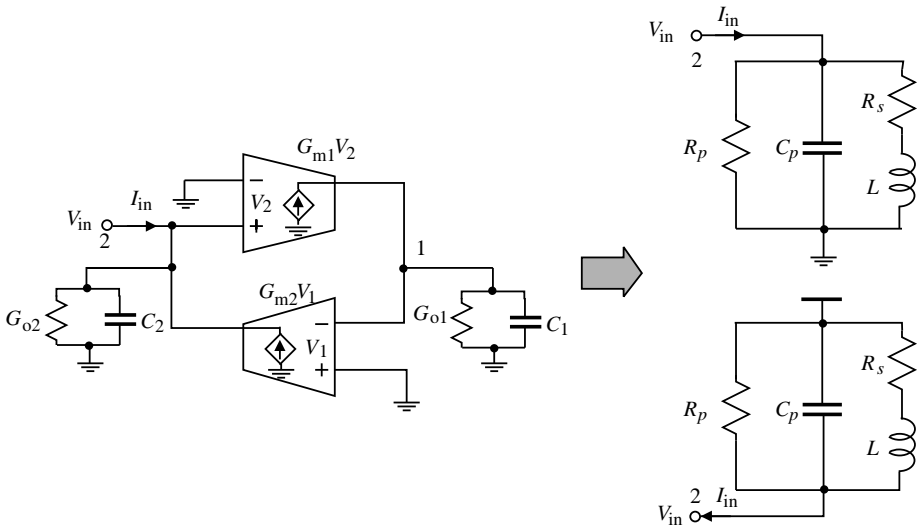


Figure 2.4. lossy single-ended gyrator-C active inductors. C_1 and G_{o1}, C_2 and G_{o2} denote the total capacitances and conductances at nodes 1 and 2, respectively.

We comments on the preceding results :

- When the input and output conductances of the transconductors are considered, the gyrator-C network behaves as a lossy inductor with its parasitic parallel resistance R_p, parallel capacitance C_p, and series resistance R_s. R_p should be maximized while R_s should be minimized to low the ohmic loss. The finite input and output impedances of the transconductors of the gyrator-C network, however, have no effect on the inductance of the active inductor.

- R_p and C_p are solely due to G_{o2} and C_2. G_{o1} and C_1 only affect R_s and L.

- The resonant frequency of the RLC networks of the active inductor is given by

$$\omega_o = \frac{1}{LC_p} = \sqrt{\frac{G_{m1}}{C_1}\frac{G_{m2}}{C_2}} = \sqrt{\omega_{t1}\omega_{t2}}, \tag{2.10}$$

  where

$$\omega_{t1,2} = \frac{G_{m1,2}}{C_{1,2}} \tag{2.11}$$

  is the cut-off frequency of the transconductors. ω_o is the self-resonant frequency of the gyrator-C active inductor. This self-resonant frequency is typically the maximum frequency at which the active inductor operates. The self-resonant frequency of an active inductor is set by the cut-off frequency of the transconductors constituting the active inductor.

- The small-signal behavior of a gyrator-C active inductor is fully characterized by its RLC equivalent circuit. The RLC equivalent circuit of gyrator-C active inductors, however, can not be used to quantify the large-signal behavior, such as the dependence of the inductance on the dc biasing condition of the transconductors and the maximum signal swing of the gyrator-C active inductors.

- When the conductances encountered at nodes 1 and 2 of the gyrator-C active inductors are zero (lossless), the phase of the impedance of the synthesized inductor is $\frac{\pi}{2}$. However, when these conductances are non-zero, the phase of the impedance of the synthesized inductor will deviate from $\frac{\pi}{2}$, giving rise to a phase error. The phase error is due to R_p and R_s of the active inductors. The phase of the impedance of practical active inductors should be made constant and to be as close as possible to $\frac{\pi}{2}$.

- The finite input and output impedances of the transconductors constituting active inductors result in a finite quality factor. For applications such as band-pass filters, active inductors with a large quality factor are mandatory. In these cases, Q-enhancement techniques that can offset the detrimental effect of R_p and R_s should be employed to boost the quality factor of the active inductors.

2.1.4 Lossy Floating Gyrator-C Active Inductors

Lossy floating gyrator-C active inductors can be analyzed in a similar way as lossy single-ended gyrator-C active inductors. Consider the lossy floating gyrator-C network shown in Fig.2.5. We continue to assume that the transconductances of the transconductors are constant. Writing KCL at nodes 1-, 1+, 2-, and 2+ yields

$$\begin{aligned} &-G_{m1}(V_2^+ - V_2^-) + \Big(\frac{sC_1 + G_{o1}}{2}\Big)(V_1^- - V_1^+) = 0, \\ &I_{in} + \Big(\frac{sC_2 + G_{o2}}{2}\Big)(V_2^- - V_2^+\Big) + G_{m2}(V_1^+ - V_1^-) = 0, \end{aligned} \tag{2.12}$$

The admittance looking into port 2 of the gyrator-C network is obtained from

$$\begin{aligned} Y &= \frac{I_{in}}{V_2^+ - V_2^-} \\ &= s\frac{C_2}{2} + \frac{G_{o2}}{2} + \frac{1}{s\Big(\frac{C_1}{2G_{m1}G_{m2}}\Big) + \frac{G_{o1}}{2G_{m1}G_{m2}}}. \end{aligned} \tag{2.13}$$

Eq.(2.12) can be represented by the RLC network shown in Fig.2.5 with its parameters given by

$$\begin{aligned} R_p &= \frac{2}{G_{o2}}, \\ C_p &= \frac{C_2}{2}, \\ R_s &= \frac{G_{o1}/2}{G_{m1}G_{m2}}, \\ L &= \frac{C_1/2}{G_{m1}G_{m2}}. \end{aligned} \tag{2.14}$$

The constant 2 in (2.14) is due to the floating configuration of the active inductor. The capacitance and conductance at the interface nodes $1+$ and $1-$ and those at the internal nodes $2+$ and $2-$ will become $C_2/2$ and $G_{o2}/2$, and $C_1/2$ and $G_{o21}/2$, respectively. Eq.(2.9) can be used to derive (2.14) without modification.

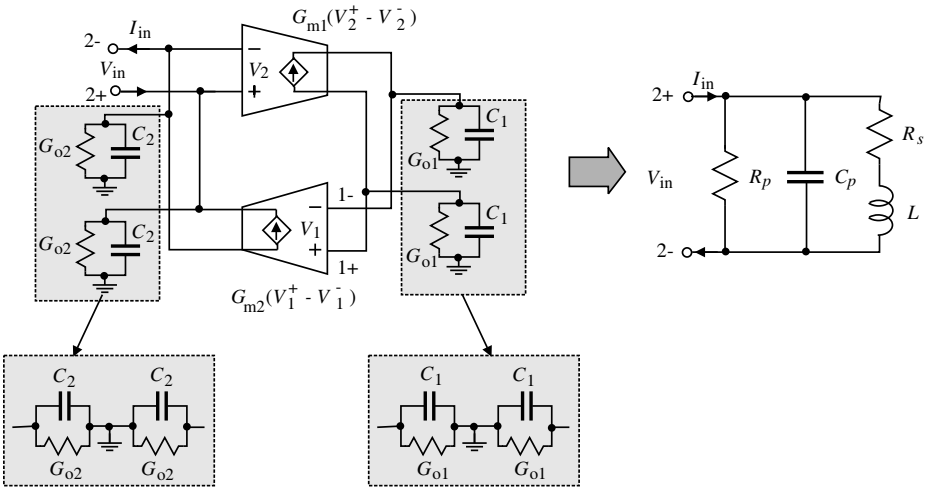


Figure 2.5. Lossy floating gyrator-C active inductors. C_1 and G_{o1}, C_2 and G_{o2} represent the total capacitances and conductances at nodes 1 and 2, respectively.

2.2 Characterization of Active Inductors

In this section, we investigate the most important figure-of-merits that provide quantitative measures of the performance of active inductors. These figure-of-merits include frequency range, inductance tunability, quality factor, noise, linearity, stability, supply voltage sensitivity, parameter sensitivity, signal sensitivity, and power consumption.

2.2.1 Frequency Range

It was shown in the preceding section that an lossless gyrator-C active inductor exhibits an inductive characteristic across the entire frequency spectrum. A lossy gyrator-C active inductor, however, only exhibits an inductive characteristic over a specific frequency range. This frequency range can be obtained by examining the impedance of the RLC equivalent circuit of the lossy active inductor

$$Z = \left(\frac{R_s}{C_p L}\right) \frac{s\frac{L}{R_s} + 1}{s^2 + s\left(\frac{1}{R_p C_p} + \frac{R_s}{L}\right) + \frac{R_p + R_s}{R_p C_p L}}. \tag{2.15}$$

When complex conjugate poles are encountered, the pole resonant frequency of Z is given by

$$\omega_p = \sqrt{\frac{R_p + R_s}{R_p C_p L}}. \tag{2.16}$$

Because $R_p \gg R_s$, Eq.(2.16) is simplified to

$$\omega_p \approx \sqrt{\frac{1}{LC_p}} = \omega_o, \tag{2.17}$$

where ω_o is the self-resonant frequency of the active inductor. Also observe that Z has a zero at frequency

$$\omega_z = \frac{R_s}{L} = \frac{G_{o1}}{C_1}. \tag{2.18}$$

The Bodé plots of Z are sketched in Fig.2.6. It is evident that the gyrator-C network is resistive when $\omega < \omega_z$, inductive when $\omega_z < \omega < \omega_o$, and capacitive when $\omega > \omega_o$. The frequency range in which the gyrator-C network is inductive is lower-bounded by ω_z and upper-bounded by ω_o. Also observed is that R_p has no effect on the frequency range of the active inductor. R_s, however, affects the lower bound of the frequency range over which the gyrator-C network is inductive. The upper bound of the frequency range is set by the self resonant frequency of the active inductor, which is set by the cut-off frequency of the transconductors constituting the active inductor. For a given inductance L, to maximize the frequency range, both R_s and C_p should be minimized.

2.2.2 Inductance Tunability

Many applications, such as filters, voltage or current controlled oscillators, and phase-locked loops, require the inductance of active inductors be tunable with a large inductance tuning range. It is seen from (2.9) that the inductance of gyrator-C active inductors can be tuned by either changing the load capacitance or varying the transconductances of the transconductors constituting the active inductors. Capacitance tuning in standard CMOS technologies is usually done by using varactors. Two types of varactors exists, namely pn-junction varactors

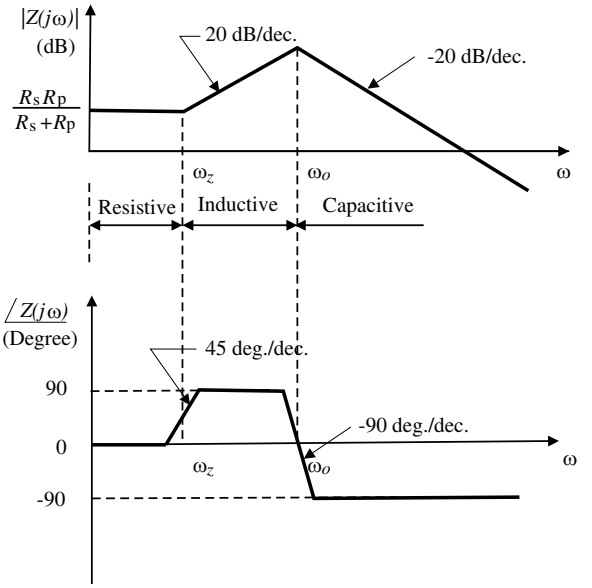


Figure 2.6. Bodé plots of the impedance of lossy gyrator-C active inductors.

and MOS varactors. The sideviews of pn-junction varactors are shown in Fig.2.7 for p+/n-well junctions and Fig.2.8 for n+/p-well junctions. Because p-substrate is connected to the ground, n+/p-well varactors are single-ended. p+/n-well varactors, on the other hand, are floating varactors. The swing of the voltages at the nodes of the varactors must ensure that the n+/p-well and p+/n-well junctions be revise biased all the time such that a junction capacitance exists. The junction capacitance of an abrupt pn-junction is given by

$$C_J = \frac{C_{Jo}}{\sqrt{1 + \dfrac{v_R}{\phi_o}}}, \tag{2.19}$$

where C_{Jo} is the junction capacitance at zero-biasing voltage, v_R is the reverse biasing voltage of the junction and ϕ_o is built-in potential of the junction. It is seen that C_J varies with v_R in a nonlinear fashion. The performance of junction varactors is affected by the following factors :

- Large parasitic series resistance - p+/n-well varactors suffer from a large series resistance - the resistance of the n-well. As a result, the quality factor of the varactor quantified by

$$Q = \frac{1}{\omega R_{n-well} C}, \tag{2.20}$$

where R_{n-well} is the parasitic series resistance, is small. To minimize this unwanted resistance, the spacing between p+ and n+ diffusions should be minimized.

- Large parasitic capacitance between n-well and p-substrate - The larger the capacitance of the varactors, the larger the n-well and subsequently the larger the n-well/p-substrate junction capacitance.
- Small capacitance tuning range - The nonlinear characteristics of C_J result in a small capacitance tuning range with a low capacitance tuning ratio.
- Stringent voltage swing requirement - As pointed out earlier that the p+/n-well and n+/p-well junctions must remain in a reverse biasing condition all the time to ensure the existence of a junction capacitance. This imposes a stringent constraint on the swing of the voltage across the terminals of the varactors

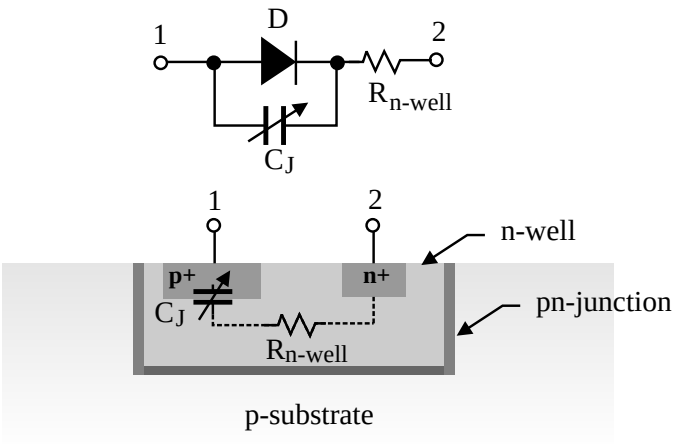


Figure 2.7. Sideview of p+/n-well varactors

The sideview of accumulation-mode MOS varactors is shown in Fig.2.9 for $V_G < V_S$ and Fig.2.10 for $V_G > V_S$. If $V_G < V_S$, the electrons in the n-well region underneath the gate will be repelled and a depletion region is created. When $V_G > V_S$, the electrons from the n+ diffusion regions will be pulled to the region underneath the gate, creating an accumulation layer and C_{GS} arises to the gate-oxide capacitance. As pointed out in [68] that $\frac{C_{max}}{C_{min}}$ can be made from 2.5 to 3 when $-1V \leq v_{GS} \leq 1V$. A key advantage of accumulation-mode MOS varactors is the large voltage swing across the terminals of the varactors. They are the most widely used varactors in voltage/current-controlled oscillators.

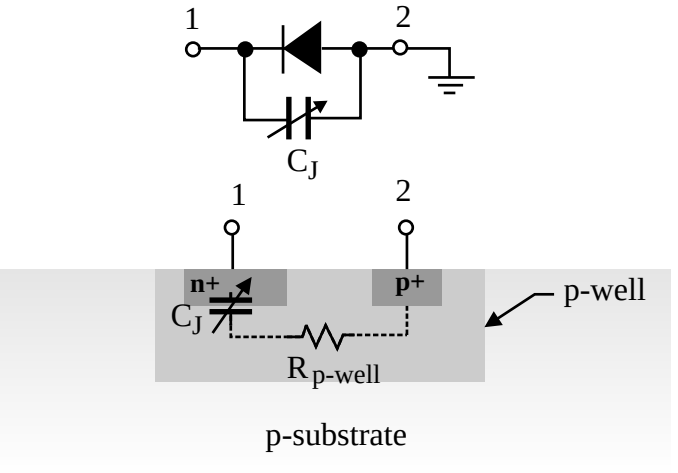


Figure 2.8. Sideview of n+/p-well varactors.

A common drawback of junction varactors and MOS varactors is their small capacitance tuning range.

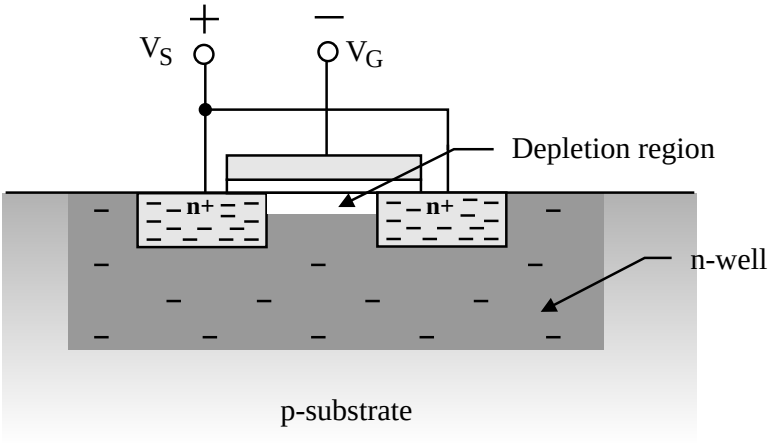


Figure 2.9. Sideview of accumulation-mode MOS varactors when $V_G < V_S$.

Conductance tuning can be done by varying the dc operating point of the transconductors. This approach offers a large conductance tuning range, subsequently a large inductance tuning range. The conductance tuning range is set by the constraint that the transconducting transistors of the transconductors must remain in the saturation. Conductance tuning can be used for the coarse tuning of the inductance while capacitance tuning can be used for the fine tuning of the inductance, as shown in Fig.2.12. The conductance of either the transconductor

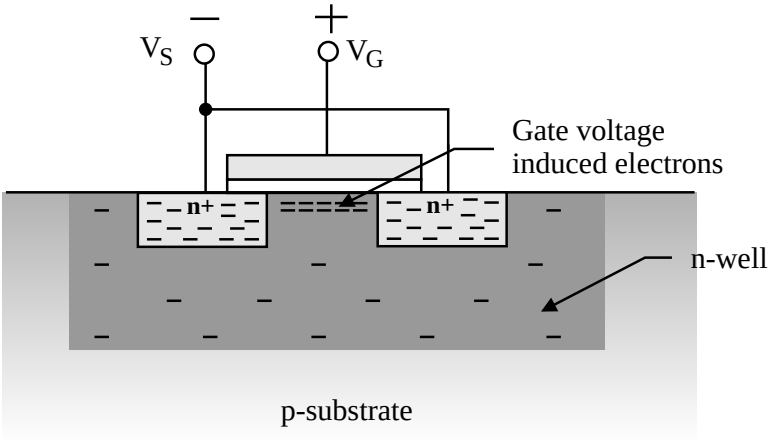


Figure 2.10. Sideview of accumulation-mode MOS varactors when $V_G > V_S$.

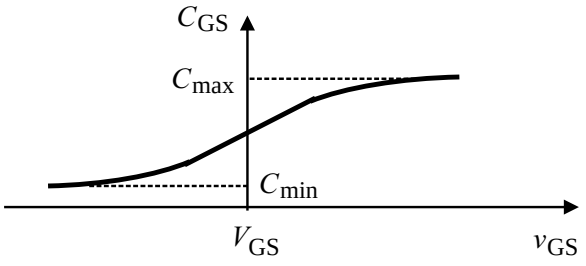


Figure 2.11. Capacitance of accumulation-mode MOS varactors.

with a positive transconductance or that with a negative transconductance can be tuned. The conductance tuning range is set by the pinch-off condition while the capacitance tuning range is set by the range of the control voltage of the varactors.

It is seen from (2.9) that a change in the transconductances of the transconductors of an active inductor will not affect R_p and C_p of gyrator-C active inductors. It will, however, alter the parasitic series resistance R_s of the active inductor. This is echoed with a change in the quality factor of the active inductors. The variation of the quality factor due to the tuning of L must therefore be compensated for such that L and Q are tuned in a truly independent fashion. It should be noted that the fine tuning of the inductance of active inductors from the capacitance tuning does not affect R_s.

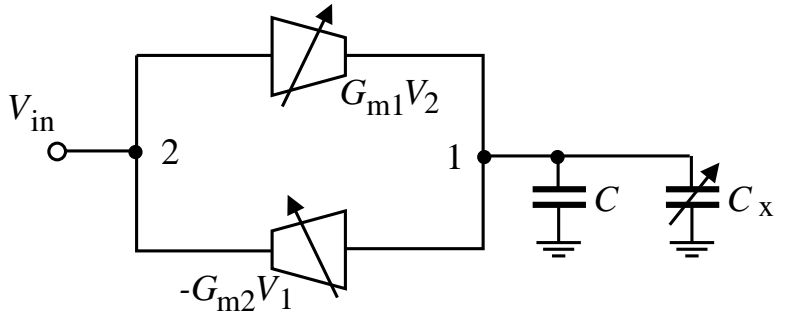


Figure 2.12. Inductance tuning of gyrator-C active inductors. Conductance tuning can be carried out by varying either G_{m1} or G_{m2} while capacitance tuning is done by varying the varactor C_x.

2.2.3 Quality Factor

The quality factor Q of an inductor quantifies the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle. For spiral inductors, the quality factor of these inductors is independent of the voltage / current of the inductors. This property, however, does not hold for active inductors as the inductance of these inductors depends upon the transconductances of the transconductors constituting the active inductors and the load capacitance. When active inductors are used in applications such as LC oscillators, the inductance of the active inductors is a strong function of the swing of the voltage and current of the oscillators. To quantify the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle and relate it to the performance of LC oscillators, in particular, the phase noise of the oscillators, an alternative definition of the quality factor that accounts for the swing of the voltage / current of the active inductors is needed.

Instantaneous Quality Factor

The quality factor Q of an inductor quantifies the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle [33, 29]

$$Q = 2\pi \times \frac{\text{Net magnetic energy stored}}{\text{Energy dissipated in one oscillation cycle}}. \qquad (2.21)$$

For a linear inductor, the complex power of the active inductor is obtained from

$$P(j\omega) = I(j\omega)V^*(j\omega) = \Re e[Z]|I(j\omega)|^2 + j\Im m[Z]|I(j\omega)|^2, \qquad (2.22)$$

where $\Re e[Z]$ and $\Im m[Z]$ are the resistance and inductive reactance of the inductor, respectively, $V(j\omega)$ and $I(j\omega)$ are the voltage across and the current through the inductor, respectively, the superscript $*$ is the complex conjugation operator, and $|.|$ is the absolute value operator. The first term in (2.22) quantifies the net energy loss arising from the parasitic resistances of the inductor, whereas the second term measures the magnetic energy stored in the inductor. Eq.(2.21) in this case becomes

$$Q = \frac{\Im m[Z]}{\Re e[Z]}. \tag{2.23}$$

Eq.(2.23) provides a convenient way to quantify Q of linear inductors including active inductors.

Active inductors are linear when the swing of the voltages / currents of the inductors are small and all transistors of the active inductors are properly biased. The quality factor of a lossy gyrator-C active inductor can be derived directly from (2.15) and (2.23)

$$Q = \left(\frac{\omega L}{R_s}\right) \frac{R_p}{R_p + R_s\Big[1 + \Big(\frac{\omega L}{R_s}\Big)^2\Big]} \left[1 - \frac{R_s^2 C_p}{L} - \omega^2 L C_p\right]. \tag{2.24}$$

Fig.2.13 shows the frequency dependence of the quality factor of the active inductor with $R_s = 4\Omega$, $R_p = 1k\Omega$, $C_p = 140$ fF, and $L = 1.6$ nH [33]. It is seen that the first term in (2.24), denoted by

$$Q_1 = \frac{\omega L}{R_s}, \tag{2.25}$$

quantifies the quality factor of the active inductor at low frequencies. The second term, denoted by

$$Q_2 = \frac{R_p}{R_p + R_s\left[1 + \Big(\frac{\omega L}{R_s}\Big)^2\right]}, \tag{2.26}$$

accounts for the effect of the finite output impedance of deep sub-micron MOSFETs, whereas the third term, denoted by

$$Q_3 = 1 - \frac{R_s^2 C_p}{L} - \omega^2 L C_p, \tag{2.27}$$

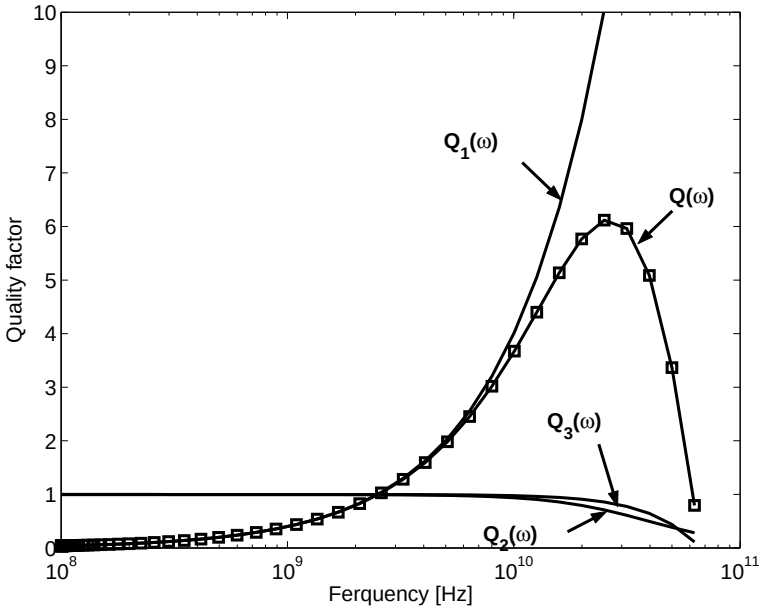


Figure 2.13. Frequency dependence of the quality factor of active inductors.

shows that the quality factor vanishes when frequency approaches the cut-off frequency of the transconductors of the active inductor. Q_2 and Q_3 manifest themselves at high frequencies only.

The sensitivity of the quality factor of the active inductor with respect to R_s and R_p is investigated in Figs.2.14 and 2.15, respectively. It is seen that Q_1 dominates the quality of the active inductor and is therefore widely used to quantify the quality factor of active inductors.

To boost the quality factor of active inductors, R_s must be minimized. Four approaches can be used to reduce R_s:

- *Approach 1* - Because $R_s = \dfrac{G_{o1}}{G_{m1}G_{m2}}$, R_s can be lowered by reducing G_{o1} directly. Since G_{o1} is typically the output impedance of the transconductor with a positive transconductance, the use of transconductors with a large output impedance is critical. As an example, consider the transconductors shown in Fig.2.16. The transconductance of the transconductor in Fig.2.16(a) is positive. This is because an increase in v_{in} will lead to an increase in v_{GS}, which in turn increases i_D. Because $i_o = i_D - J$, i_o will increase as well. The transconductance of the transconductor in Fig.2.16(b) is also positive. This is because an increase in v_{in} will decrease i_{D1}. As a result, $i_{D2} = J_1 - i_{D1}$ will increase. Since $i_o = i_{D2} - J_2$, i_o will increase as well. Although both transconductors have a positive transcon-

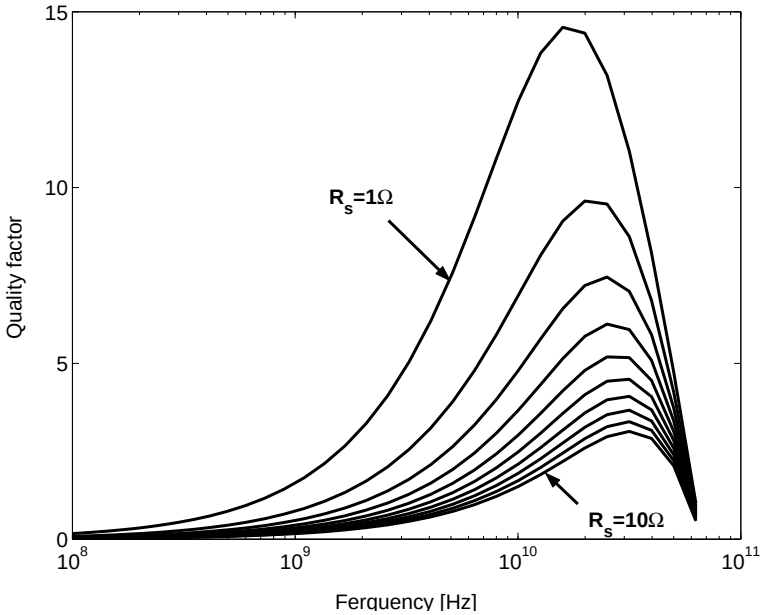


Figure 2.14. The effect of R_s on the quality factor of active inductors. R_s is varied from 1Ω to 10Ω with step 1Ω.

ductance and both have an infinite input impedance, the output impedance of the transconductor in Fig.2.16(a) is given by $\frac{1}{g_m}$ approximately whereas that of the transconductor in Fig.2.16(b) is given by r_{o2}. Active inductors constructed using the transconductor in Fig.2.16(b) will have a smaller R_s, subsequently a higher Q.

- *Approach 2* - R_s can be lowered by increasing G_{m1} and G_{m2} directly. Since the transconductances of the transconductors are directly proportional to the dc biasing currents and the width of the transistors of the transconductors, R_s can be lowered by either increasing the dc biasing currents or increasing the transistor width. The former, however, increases the static power consumption of the active inductors whereas the latter lowers the self-resonant frequency of the active inductors. Another downside of this approach is that the inductance of the inductors L will also be affected.

- *Approach 3* - Reduce G_{o1} using advanced circuit techniques, such as cascodes. Cascodes are effective in lowering the output conductance and can be used here to reduce G_{o1}, as shown in Fig.2.17. Table 2.1 compares the minimum supply voltage and output conductance of basic, cascode, regulated cascode, and multi-regulated cascode transconductors.

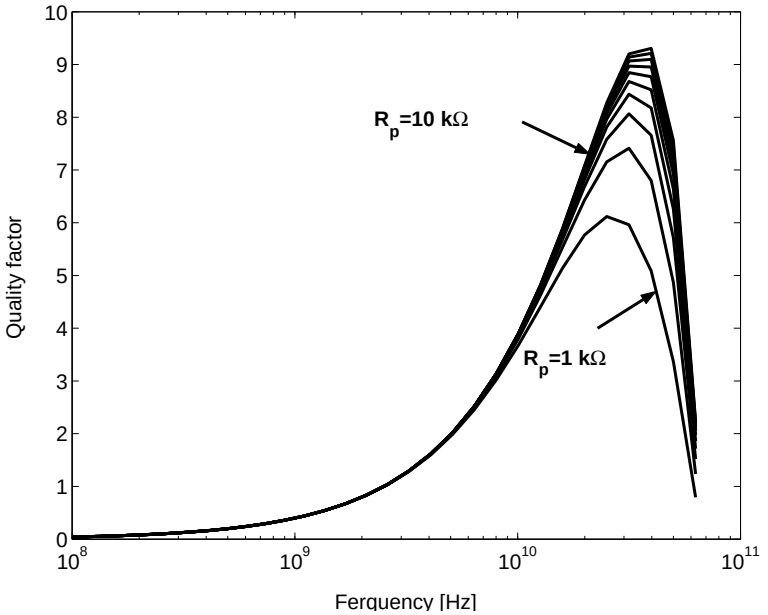


Figure 2.15. The effect of R_p on the quality factor of active inductors. R_p is varied from 1kΩ to 10kΩ with step 1kΩ.

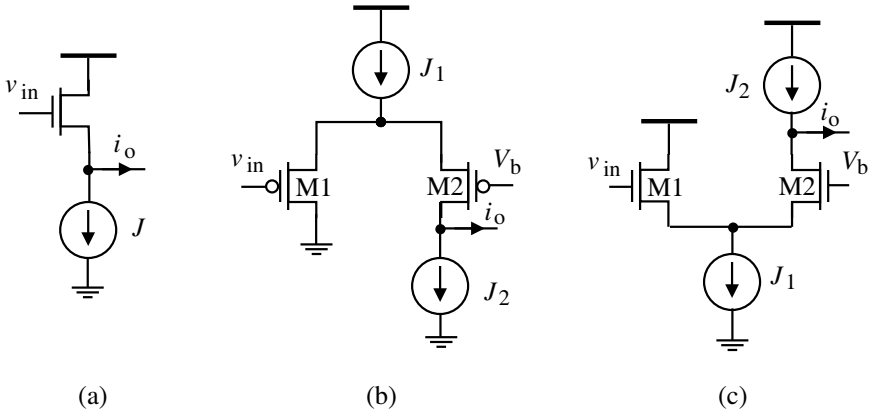


Figure 2.16. Simplified schematics of transconductors with a positive transconductor. (a) Common-drain transconductor; (b,c) Differential-pair transconductors.

- *Approach 4* - Use a shunt negative resistor at the output of the positive transconductor to cancel out the parasitic resistances, both series and parallel, of active inductors. It is well known that the series RL network of the RLC network shown in Fig.2.18 can be replaced with the parallel RL network shown in the figure with [68]

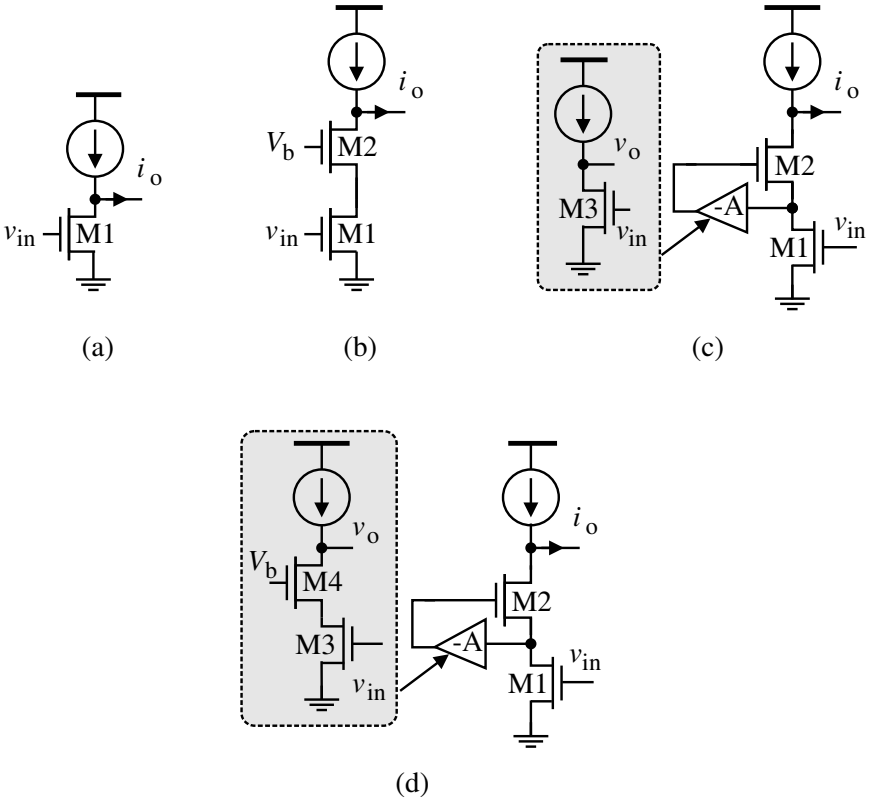


Figure 2.17. Simplified schematics of cascode transconductors. (a) Basic transconductor; (b) Cascode transconductor; (c) Regulated cascode transconductor; (d) Multi-regulated cascode transconductor.

$$\begin{aligned} R_p &= R_s(1+Q^2) \\ L_p &= L_s\Big(1+\frac{1}{Q^2}\Big), \end{aligned} \tag{2.28}$$

where $Q = \dfrac{\omega L_s}{R_s}$. This is because in order to have the two network to be equivalent, in other words, to exhibit the same terminal impedance, $Z_s(j\omega) = Z_p(j\omega)$ is required.

$$R_s + j\omega L_s = \frac{j\omega R_p L_p}{R_p + j\omega L_p}. \tag{2.29}$$

Matching the real and imaginary parts yield

Table 2.1. The minimum supply voltage and output conductance of basic and cascode transconductors.

Transconductor	Min. V_{DD}	Output impedance
Basic	$2V_{sat}$	$G_o = \frac{1}{r_o}$
Cascode	$3V_{sat}$	$G_o = \frac{1}{r_{o1}(r_{o2}g_{m2})}$
Regulated cascode	$2V_T + V_{sat}$	$G_o = \frac{1}{r_{o1}(r_{o2}g_{m2})(r_{o3}g_{m3})}$
Multi-regulated cascode	$2V_T + V_{sat}$	$G_o = \frac{1}{r_{o1}(r_{o2}g_{m2})(r_{o3}g_{m3})(r_{o4}g_{m4})}$.

$$\begin{aligned} R_s R_p - \omega^2 L_s L_p &= 0, \\ R_s L_p + R_p L_s &= R_p L_p. \end{aligned} \tag{2.30}$$

Eq.(2.28) follows from Eq.(2.30). Note that (2.28) is valid at all frequencies.

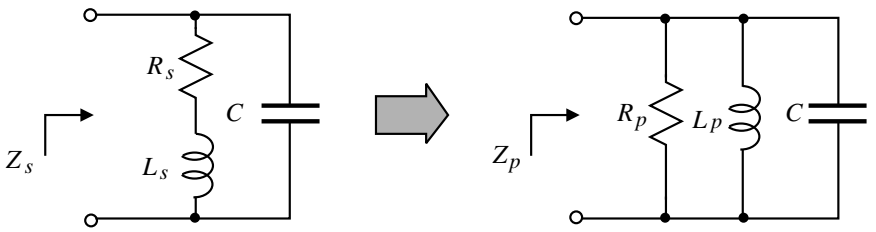


Figure 2.18. Transformation of a RL parallel branch to a RL series branch.

Now consider the RLC network of an active inductor shown in Fig.2.19. The $L \sim R_s$ branch of the RLC circuit of the active inductor is replaced with the parallel $\hat{L} \sim \hat{R}_p$ network with

$$\begin{aligned} \hat{L} &= L\Big(1 + \frac{1}{Q^2}\Big), \\ \hat{R}_p &= R_s(1 + Q^2). \end{aligned} \tag{2.31}$$

Consider two cases :

– Case 1 - If R_s is negligible, the quality factor of the active inductor is mainly determined by R_p. From (2.24) with $R_s = 0$, we arrive at

$$Q = \frac{R_p}{\omega L}\left[1 - \left(\frac{\omega}{\omega_o}\right)^2\right]. \tag{2.32}$$

At frequencies below ω_o, $\left(\frac{\omega}{\omega_o}\right)^2 \approx 0$ and

$$Q \approx \frac{R_p}{\omega L_s} \tag{2.33}$$

follows.

– Case 2 - If R_p is large, the quality factor is mainly determined by R_s

$$Q = \frac{\omega L}{R_s}\left[1 - \left(\frac{\omega_z}{\omega_o}\right)^2 - \left(\frac{\omega}{\omega_o}\right)^2\right]. \tag{2.34}$$

At frequencies above ω_z and below ω_o, $\left(\frac{\omega_z}{\omega_o}\right)^2 \approx 0$ and $\left(\frac{\omega}{\omega_o}\right)^2 \approx 0$. Eq.(2.34) is simplified to

$$Q \approx \frac{\omega L}{R_s}. \tag{2.35}$$

As shown in Fig.2.19, the total parasitic parallel resistance of the active inductor becomes

$$R_{total} = R_p // \hat{R}_p. \tag{2.36}$$

In this case, a negative resistor of resistance $R_{comp} = -R_{total}$ can be connected in parallel with C_p to eliminate the effect of both R_p and R_s of the active inductor simultaneously. Note that the resistance of the negative resistor should be made tunable such that a total cancellation can be achieved. The quality factor of the compensated active inductor at ω_o is given by

$$Q(\omega_o) = (R_p || \hat{R}_p || R_{comp}) \sqrt{\frac{C_p + C_{comp}}{\hat{L}}}, \tag{2.37}$$

where C_{comp} is the input capacitance of the compensating negative resistor. It should be noted that because R_s and R_p are frequency-dependent, R_{comp} should be designed in such a way that a total resistance cancellation is achieved across the frequency range of the active inductor. It should also be noted that although the negative resistor compensation technique is widely used to improve the quality factor of spiral inductors, a total compensation in this case is difficult to achieve. This is because an active negative resistor is used to cancel out the largely skin-effect induced parasitic series resistance of spirals.

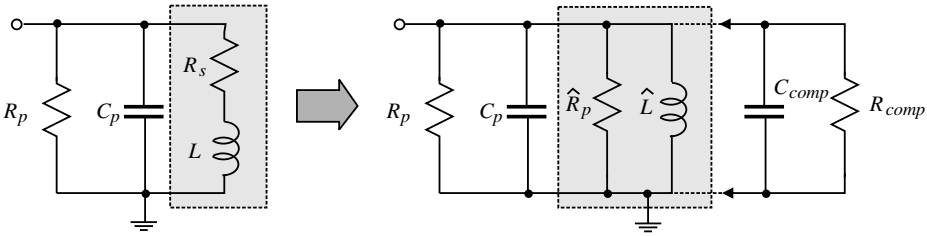


Figure 2.19. Q enhancement using a shunt negative resistor.

Average Quality Factors

Active inductors are RLC tanks when R_s, R_p, and C_p are accounted for. The quality factor of LC tanks is obtained from [69]

$$Q(\omega) = \frac{\omega_o}{2} \frac{\partial \phi(\omega)}{\partial \omega}, \tag{2.38}$$

where $\phi(\omega)$ is the phase of the tank impedance. The quality factor of a passive LC tank at a given frequency is independent of the current of the tank.

Unlike passive LC tanks, the inductance of the active inductors varies with the current / voltage of the inductors. The effective quality factor defined as

$$\overline{Q(\omega)} = \frac{\omega}{2(I_{max} - I_{min})} \int_{I_{min}}^{I_{max}} Q(\omega, i) di, \tag{2.39}$$

where I_{min} and I_{max} are the minimum and maximum currents of the transconductors of active inductors, and $Q(\omega_o, i)$ is the instantaneous quality factor at frequency ω and channel current i provides an effective mean to quantify the quality factor of active inductors, especially when active inductors are employed in circuits that are operated in a large-signal mode, such as LC tank oscillators.

2.2.4 Noise

Active inductors exhibit a high level of noise as compared with their spiral counterparts. To analyze the noise of a gyrator-C active inductor, the power of the input-referred noise-voltage and that of the noise-current generators of the transconductors constituting the active inductor must be derived first. Fig.2.20 shows the partial schematics of basic transconductors widely used in the construction of gyrator-C active inductors. The power of the input-referred noise-voltage generator, denoted by $\overline{v_n^2}$, and that of the input-referred noise-current generator, denoted by $\overline{i_n^2}$, of these transconductors can be derived using conventional noise analysis approaches for 2-port networks [70], and the results are given in Table 2.2 where

$$\overline{i_{nD}^2} = 4kT(\gamma + R_g g_m) g_m \Delta f \tag{2.40}$$

represents the sum of the power of the thermal noise generated in the channel of MOSFETs and the thermal noise of the gate series resistance of MOSFETs, R_g is the gate series resistance, $\gamma = 2.5$ for deep sub-micron devices, T is the temperature in degrees Kelvin, and k is Boltzmann constant. The effect of the flicker noise of MOSFETs, which has a typical corner frequency of a few MHz [71], is neglected. The thermal noise of other parasitics of MOSFETs, such as the thermal noise of the bulk resistance of the source and drain diffusions, is also neglected.

To illustrate how the results of Table 2.2 are derived, consider the common-gate transconductor. To derive the input-referred noise-voltage generator $\overline{v_n^2}$ of the transconductor, we first short-circuit the input of the transconductor, as shown in Fig.2.21.

The output noise power of the transconductor due to i_{nD} is calculated

$$\overline{v_{no}^2} = r_o^2 \overline{i_{nD}^2}, \tag{2.41}$$

where r_o is the output resistance of the transistor. We then remove $\overline{i_{nD}^2}$ and apply v_n at the input of the transconductor, as shown in Fig.2.22. The output noise power of the transconductor is obtained

$$\overline{v_{no}^2} = (1 + g_m r_o)^2 \overline{v_n^2}. \tag{2.42}$$

Equating (2.41) and (2.42) yields

$$\overline{v_n^2} = \frac{r_o^2}{(1 + g_m r_o)^2} \overline{i_{nD}^2} \approx \frac{1}{g_m^2} \overline{i_{nD}^2}. \tag{2.43}$$

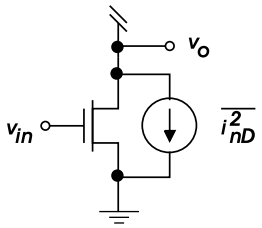
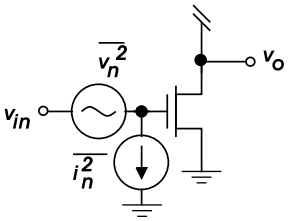
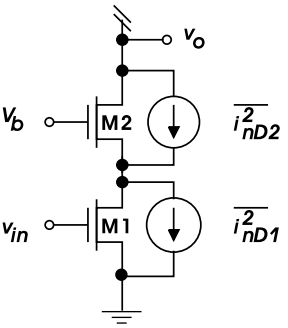
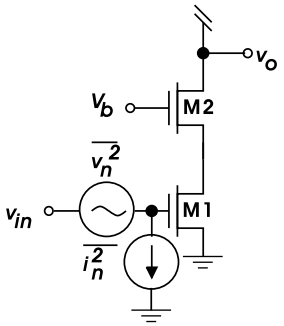
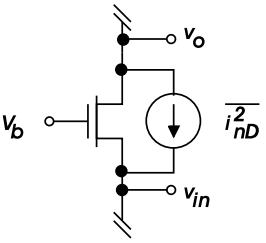
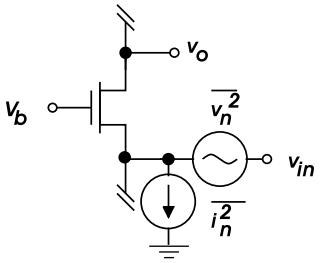
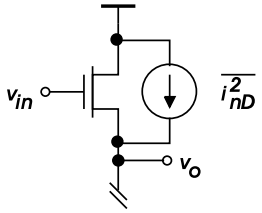
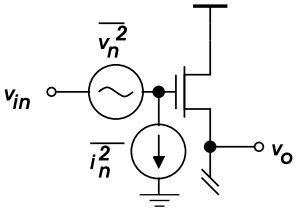
	Transconductors with noise sources	Transconductors with noise generators
Common source		
Cascode		
Common gate		
Source follower		

Figure 2.20. Input-referred noise-voltage and noise-current generators of transconductors at low frequencies.

Table 2.2. Power of input-referred noise-voltage and noise-current generators of basic transconductors at low frequencies.

Transconductor	$\overline{v_n^2}$	$\overline{i_n^2}$
Common source	$\overline{v_n^2} = \frac{\overline{i_{nD}^2}}{g_m^2}$	$\overline{i_n^2} = 0$
Cascode	$\overline{v_n^2} = \frac{\overline{i_{nD1}^2}}{g_{m1}^2} + \frac{\overline{i_{nD2}^2}}{(g_{m1} r_{o1} g_{m2})^2}$	$\overline{i_n^2} = 0$
Common gate	$\overline{v_n^2} = \frac{\overline{i_{nD}^2}}{g_m^2}$	$\overline{i_n^2} = 0$
Source follower	$\overline{v_n^2} = \frac{\overline{i_{nD}^2}}{g_m^2}$	$\overline{i_n^2} = 0$

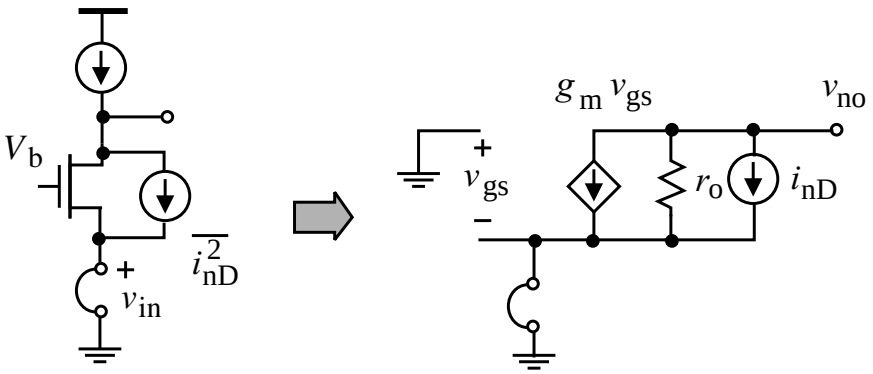


Figure 2.21. Derivation of input-referred noise-voltage generator of a common-gate transconductor at low frequencies.

Note that we have utilized $r_o g_m \gg 1$ in (2.43) to simplify the results.

To derive the noise-current generator of the common-gate transconductor, consider Fig.2.23 where the input port of the transconductor is open-circuited and the output noise power of the circuit is calculated. To avoid the difficulty caused by the floating node 1, we assume that there exists a resistor of resistance

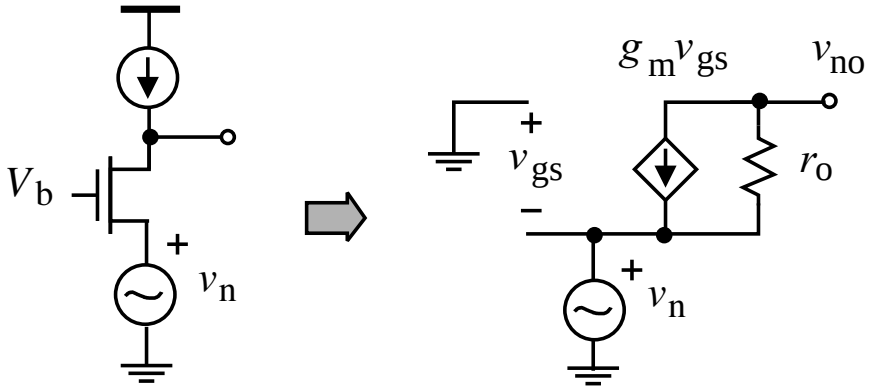


Figure 2.22. Derivation of the input-referred noise-voltage generator of a common-gate transconductor at low frequencies.

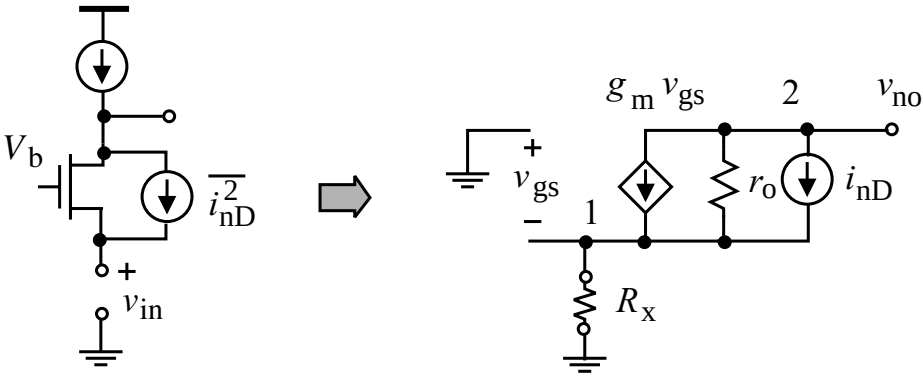


Figure 2.23. Derivation of the input-referred noise-current generator of a common-gate transconductor at low frequencies.

R_x between node 1 and the ground. Note that this approach is used in most IC CAD systems to avoid floating nodes. Writing KCL at nodes 1 and 2 yields

$$\begin{aligned}(g_x + g_m + g_o)v_1 - g_o v_2 &= i_{nD} \quad \text{(node 1)},\\ -(g_o + g_m)v_1 + g_o v_2 + i_{nD} &= 0 \quad \text{(node 2)}.\end{aligned} \tag{2.44}$$

Solving (2.44) yields

$$\overline{v_2^2} = \frac{1}{g_o^2}\overline{i_{nD}^2}. \tag{2.45}$$

We then apply the noise-current generator i_n at the input of the circuit, remove all the noise sources of the circuit, as shown in Fig.2.24, and compute the output noise power. Writing KCL at nodes 1 and 2 yields

$$\begin{aligned} &(g_x + g_m + g_o)v_1 - g_o v_2 + i_n = 0 \quad \text{(node 1)}, \\ &-(g_o + g_m)v_1 + g_o v_2 = 0 \qquad\qquad \text{(node 2)}. \end{aligned} \tag{2.46}$$

Solving (2.46) yields

$$\overline{v_2^2} = \left(1 + \frac{g_m}{g_o}\right)^2 \frac{1}{g_x^2} \overline{i_n^2}. \tag{2.47}$$

Equating (2.45) and (2.47) yields

$$\overline{i_n^2} = \left(\frac{g_x}{g_o}\right)^2 \frac{\overline{i_{nD}^2}}{\left(1 + \frac{g_m}{g_o}\right)^2}. \tag{2.48}$$

Taking the limit $R_x \to \infty$ or equivalently $g_x \to 0$ in (2.48), we arrive at

$$\overline{i_n^2} = 0. \tag{2.49}$$

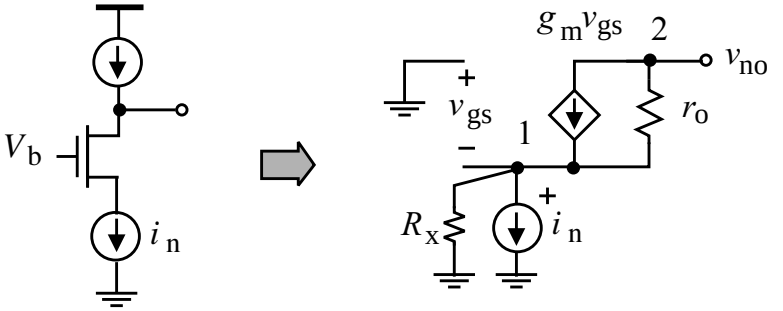


Figure 2.24. Derivation of the input-referred noise-current generator of a common-gate transconductor at low frequencies.

Once $\overline{v_n^2}$ and $\overline{i_n^2}$ of the transconductors are available, the power of the input-referred noise-voltage and noise-current generators of active inductors can be derived.

Consider the active inductor of Fig.2.25(a) where $\overline{v_{n1}^2}$ and $\overline{v_{n2}^2}$ denote the power of the noise-voltage generators of the transconductors 1 and 2, respectively, and Y_1 and Y_2 are the admittance at ports 1 and 2, respectively. For the network of Fig.2.25(a), it is trivial to show that

$$\overline{V_1^2} = \overline{\left(V_{n1} + Y_1 \frac{G_{m2}V_{n2} + Y_2 V_{n1}}{Y_1 Y_2 + G_{m1}G_{m2}} \right)^2}. \tag{2.50}$$

For the network of Fig.2.25(b), we have

$$\overline{V_1^2} = \overline{\left(V_n + \frac{Y_1}{Y_1 Y_2 + G_{m1}G_{m2}} I_n \right)^2}. \tag{2.51}$$

To ensure that Fig.2.25(a) and Fig.2.25(b) are equivalent, the right hand-side of (2.50) and that of (2.51) must be the same. To achieve this, we impose

$$\begin{aligned} V_n &= V_{n1}, \\ I_n &= Y_2 V_{n1} + G_{m2} V_{n2}. \end{aligned} \tag{2.52}$$

Because

$$Z_{in}(s) = \frac{Y_1}{Y_1 Y_2 + G_{m1}G_{m2}}, \tag{2.53}$$

we arrive at

$$V_n = V_{n1} + Z_{in} I_n. \tag{2.54}$$

For lossy gyrator-C active inductors, we have

$$\begin{aligned} Y_1 &= G_{o1} + sC_1, \\ Y_2 &= G_{o2} + sC_2, \end{aligned} \tag{2.55}$$

Eq.(2.52) becomes

$$\begin{aligned} V_n &= V_{n1}, \\ I_n &= (G_{o2} + sC_2) V_{n1} + G_{m2} V_{n2}. \end{aligned} \tag{2.56}$$

By assuming V_{n1} and V_{n2} are uncorrelated, we arrive at

$$\begin{aligned} \overline{V_n^2} &= \overline{V_{n1}^2}, \\ \overline{I_n^2} &= \left|G_{o2} + j\omega C_2\right|^2 \overline{V_{n1}^2} + G_{m2}^2 \overline{V_{n2}^2}. \end{aligned} \tag{2.57}$$

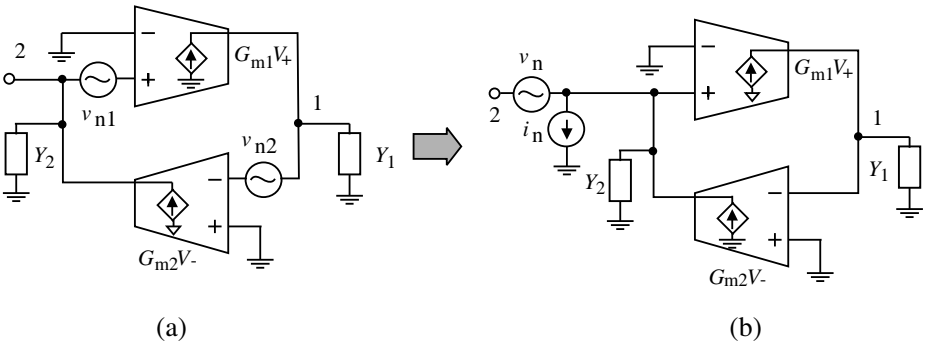


Figure 2.25. Noise of single-ended gyrator-C active inductors.

2.2.5 Linearity

The preceding development of gyrator-C active inductors assumes that the transconductors of the active inductors are linear. This assumption is only valid if the swing of the input voltage of the transconductors is small. When the voltage swing is large, the transconductors will exhibit a nonlinear characteristic and the synthesized active inductors are no longer linear. The linearity constraint of active inductors sets the maximum swing of the voltage of the active inductors. If we assume that the transconductances of the transistors of gyrator-C active inductors are constant when the transistors are biased in the saturation, then the maximum swing of the voltage of the active inductors can be estimated from the pinch-off condition of the transistors. When the transistors of active inductors enter the triode region, the transconductances of the transistors decrease from g_m (saturation) to g_{ds} (triode) in a nonlinear fashion, as illustrated graphically in Fig.2.26. It should be emphasized that although the transconductances of the transconductors of gyrator-C networks drop when the operating point of the transistors of the transconductors moves from the saturation region to the triode region, the inductive characteristics at port 2 of the gyrator-C network remain. The inductance of the gyrator-C active inductors, however, increases from $L = \dfrac{C}{G_{m1}G_{m2}}$ to $L = \dfrac{C}{G_{ds1}G_{ds2}}$, where $G_{m1,m2}$ are the transconductances of transconductors 1 and 2 respectively when

in the saturation and $G_{ds1,ds2}$ are the transconductances of transconductors 1 and 2 respectively when in the triode. Note that we have assumed the load capacitance C remains unchanged. The inductance thus varies with the swing of the voltage of the active inductors in a nonlinear fashion. It should also be noted that the parasitic resistances of active inductors also vary with the voltage swing of the active inductors.

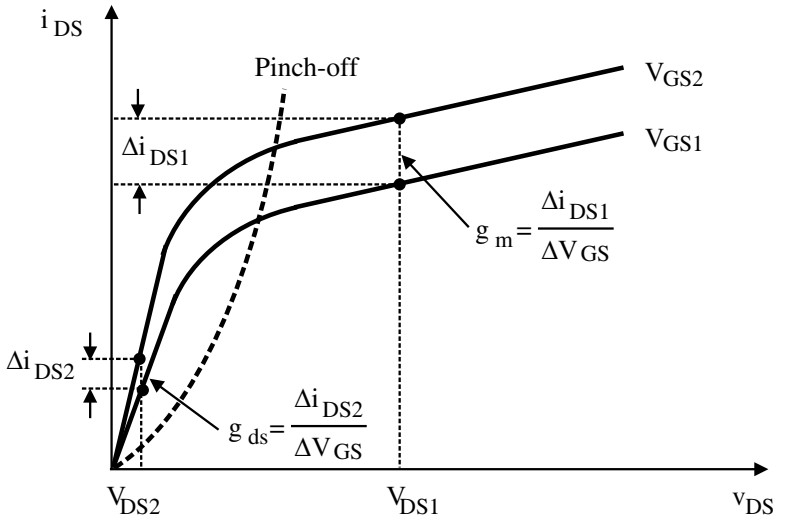


Figure 2.26. Transconductance of MOSFETs in the saturation and triode regions. Because $\Delta i_{DS1} > \Delta i_{DS2}$, $g_m > g_{ds}$ follows.

2.2.6 Stability

Gyrator-C active inductors are negative feedback systems. The stability of active inductors is critical to the overall stability of systems employing active inductors. In this section, we investigate the stability of gyrator-C active inductors.

The impedance looking into port 2 of the gyrator-C active inductor shown in Fig.2.4 is given by

$$Z = \frac{sC_1 + G_{o1}}{s^2 C_1 C_2 + s(C_1 + C_2) + G_{m1} G_{m2}}, \tag{2.58}$$

where we have utilized $G_m \gg G_o$ to simply the results. The poles of the system are given by

$$p_{1,2} = \frac{C_1 + C_2}{2C_1 C_2} \left[-1 \pm \sqrt{1 - \frac{4C_1 C_2 G_{m1} G_{m2}}{(C_1 + C_2)^2}} \right]. \tag{2.59}$$

The poles of the gyrator-C active inductor are located in the left half of the s-plane and the gyrator-C active inductor is a stable system.

The degree of stability can be assessed by evaluating its damping factor, which is obtained by comparing the denominator of (2.58) with the standard form of the characteristic equation of second-order systems

$$s^2 + 2\omega_o \xi s + \omega_o^2 = 0, \tag{2.60}$$

where ξ denotes the damping factor and ω_o is the pole resonant frequency. The result is given by

$$\xi = \frac{1}{2\sqrt{G_{m1}G_{m2}}}\left(\sqrt{\frac{C_2}{C_1}} + \sqrt{\frac{C_1}{C_2}}\right). \tag{2.61}$$

Eq.(2.61) reveals that an increase in G_{m1} and G_{m2} will lead to a decrease in ξ. This is echoed with an increase in the level of oscillation in the response of the active inductor. Also observed from (2.61) is that the ratios $\frac{C_1}{C_2}$ and $\frac{C_2}{C_1}$ have a marginal impact on the damping factor simply because these two quantities vary in the opposite directions when C_1 and C_2 change, and the values of C_1 and C_2 are often close.

If $C_1 = C_2 = C$ and $G_{m1} = G_{m2} = G_m$, we have

$$\begin{aligned} p_{1,2} &= \frac{1}{C}\Big(-1 \pm \sqrt{1 - G_m^2}\Big), \\ \xi &= \frac{1}{G_m}. \end{aligned} \tag{2.62}$$

An increase of G_m will lead to a decrease of ξ. This is echoed with a reduced level of damping. Because $\Re e[p_{1,2}] = -\frac{1}{C}$, the absolute stability margin is set by the capacitance C and is independent of G_m. It should be noted that the preceding analysis is based on the assumption that active inductors are 2nd-order systems. When the parasitics of MOSFETs are accounted for, active inductors are no longer 2nd-order systems and their stability will deteriorate.

2.2.7 Supply Voltage Sensitivity

The supply voltage sensitivity of the inductance of active inductors is a figure-of-merit quantifying the effect of the variation of the supply voltage on the inductance of the active inductors. The fluctuation of the supply voltage of a mixed analog-digital system is mainly due to the switching noise of the system

[14]. Assume that the supply voltage of a mixed-mode system containing an active inductor varies from V_{DD} and $V_{DD} + \Delta V_{DD}$, where ΔV_{DD} is a random variable with $E[\Delta V_{DD}] = 0$, where $E[.]$ denotes the mathematical mean operator. For a well designed mixed-mode system, $\Delta V_{DD} \ll V_{DD}$ holds. The small-signal analysis approach can therefore be employed to analyze the effect of ΔV_{DD} on the inductance of the active inductor. Following the definition of normalized sensitivity given in [72], the normalized sensitivity of the inductance of an active inductor to the supply voltage is defined as

$$S_{V_{DD}}^{L} = \frac{V_{DD}}{L}\frac{\partial L}{\partial V_{DD}}. \tag{2.63}$$

The fluctuation of the supply voltage V_{DD} affects the inductance of the active inductor mainly by altering the dc operating point, subsequently the transconductances of the transconductors constituting the active inductor. By assuming that the load capacitance C of the gyrator-C active inductor does not vary with V_{DD} and because $L = \dfrac{C}{G_{m1}G_{m2}}$, we arrive at

$$\frac{\partial L}{\partial V_{DD}} = -L\left(\frac{1}{G_{m1}}\frac{\partial L}{G_{m1}} + \frac{1}{G_{m2}}\frac{\partial L}{G_{m2}}\right). \tag{2.64}$$

The normalized supply voltage sensitivity of the active inductor is given by

$$S_{V_{DD}}^{L} = -\left(S_{V_{DD}}^{G_{m1}} + S_{V_{DD}}^{G_{m2}}\right), \tag{2.65}$$

where $S_{V_{DD}}^{G_{m1}}$ and $S_{V_{DD}}^{G_{m2}}$ are the normalized supply voltage sensitivity of G_{m1} and G_{m2}, respectively. Eq.(2.65) reveals that both $S_{V_{DD}}^{G_{m1}}$ and $S_{V_{DD}}^{G_{m2}}$ contribute equally to $S_{V_{DD}}^{L}$. To minimize the supply voltage sensitivity of active inductors, transconductors with a constant G_m should be used.

2.2.8 Parameter Sensitivity

The minimum feature size of MOS devices in modern CMOS technologies has been scaled down more aggressively as compared with the improvement in process tolerance such that the effect of process variation on the characteristics of circuits becomes increasingly critical. For example, the resistance of poly resistors in a typical 0.18μm CMOS process has an error of $\pm 20\%$ approximately and that of n-well resistors has an error of $\pm 30\%$ approximately. Analysis of the effect of parameter spread is vital to ensure that the performance of circuits meets design specifications once the circuits are fabricated. Active inductors consist of a number of active devices and their performance is greatly affected

by the parameter spread of these components. The normalized sensitivity of the inductance of an active inductor to a parameter x_j of the inductor defined as

$$S_{x_j}^{L} = \frac{x_j}{L}\frac{\partial L}{\partial x_j} \tag{2.66}$$

quantifies the effect of the variation of the parameter x_j on the inductance of the active inductor. By assuming that the parameters of the active inductor are Gaussian distributed and uncorrelated, the overall effect of the variation of the parameters of the active inductor on the inductance of the inductor is obtained from

$$\sigma_L^2 = \sum_{j=1}^{N} \Big(\frac{\partial L}{\partial x_j}\Big)^2 \sigma_{x_j}^2, \tag{2.67}$$

where σ_L and σ_{x_j} denote the standard deviations of L and x_j, respectively, and N is the number of the parameters of the active inductor. For a gyrator-C active inductor, because

$$\begin{aligned} \frac{\partial L}{C} &= \frac{1}{G_{m1}G_{m2}}, \\ \frac{\partial L}{G_{m1}} &= -\frac{C}{G_{m1}^2 G_{m2}}, \\ \frac{\partial L}{G_{m2}} &= -\frac{C}{G_{m1}G_{m2}^2}, \end{aligned} \tag{2.68}$$

we obtain the normalized spread of the inductance of the active inductor

$$\frac{\sigma_L^2}{L^2} = \frac{\sigma_C^2}{C^2} + \frac{\sigma_{G_{m1}}^2}{G_{m1}^2} + \frac{\sigma_{G_{m2}}^2}{G_{m2}^2}. \tag{2.69}$$

There are two ways in which circuit designers can analyze the effect of parameter spread on the inductance of active inductors, namely worst-case analysis, also known as corner analysis, and Monte Carlo analysis. The former determines the inductance of active inductors at process corners while the latter quantifies the degree of the spread of the inductance of active inductors around the nominal inductance of the inductors. The accuracy of Monte Carlo analysis increases with an increase in the number of simulation runs and is therefore

extremely time consuming. Corner analysis, on the other hand, is time-efficient but the results obtained from corner analysis are typically over conservative. Despite of this, corner analysis is the most widely used method to quantify the effect of process spread.

2.2.9 Signal Sensitivity

Unlike spiral inductors whose inductance is independent of the voltage and current of the inductors, the inductance of gyrator-C active inductors varies with the voltage and current of the transconductors constituting the active inductors. This is because the transconductances G_{m1} and G_{m2} of the transconductors are signal dependent when signal swing is large. When an active inductor is used in applications where the voltage of the active inductor experiences a large degree of variation, such as active inductor LC oscillators, the transconductances of the transconductors of the active inductor vary with the signal swing. As a result, the inductance, parasitic resistances, and quality factor of the active inductor all vary with the signal swing.

2.2.10 Power Consumption

Spiral inductors do not consume static power. Gyrator-C active inductors, however, consume dc power, mainly due to the dc biasing currents of their transconductors. The power consumption of gyrator-C active inductors themselves is usually not of a critical concern because the inductance of these inductors is inversely proportional to the transconductances of the transconductors constituting the inductors. To have a large inductance, G_{m1} and G_{m2} are made small. This is typically achieved by lowering the dc biasing currents of the transconductors. When replica-biasing is used to minimize the effect of supply voltage fluctuation on the inductance of active inductors, as to be seen shortly, the power consumed by the replica-biasing network must be accounted for. Also, when negative resistors are employed for boosting the quality factor of active inductors, their power consumption must also be included. Often the power consumption of an active inductor is set by that of its replica-biasing and negative resistor networks.

2.3 Implementation of Single-Ended Active Inductors

The need for a high self-resonant frequency of active inductors requires that the transconductors of these active inductors be configured as simple as possible. This also lowers their level of power consumption and reduces the silicon area required to fabricate the inductors. Most reported gyrator-C active inductors employ a common-source configuration as negative transconductors, common-gate, source follower, and differential pair configurations as positive

transconductors. These basic transconductors have the simplest configurations subsequently the highest cutoff frequencies and the lowest silicon consumption.

The load capacitor of the transconductors is realized using the intrinsic capacitance C_{gs} of the transistors of the transconductors directly to maximize the upper bound of the frequency range of the active inductors and to avoid the use of expensive floating capacitors, which are available only in mixed-mode CMOS processes. MOS varactors are often added in parallel with C_{gs} to tune the inductance of active inductors.

This section presents a comprehensive treatment of both the circuit implementation and characteristics of CMOS active inductors. To simplify analysis, the following assumptions are made in analysis of active inductors and in determination of both their signal swing and the minimum supply voltage : (i) nMOS and pMOS transistors have the same threshold voltage V_T. (ii) nMOS and pMOS transistors have the same pinch-off voltage V_{sat}. (iii) Only C_{gs} is considered. C_{gd} and parasitic diffusion capacitances are neglected unless otherwise noted explicitly. (iv) The minimum voltage drop across biasing current sources and current-source loads is V_{sat}.

2.3.1 Basic Gyrator-C Active Inductors

Fig.2.27 show the schematic of two basic gyrator-C active inductors. In Fig.2.27(a), the transconductor with a positive transconductance is common-gate configured while the transconductor with a negative transconductance is common-source configured. In Fig.2.27(b), the transconductor with a positive transconductance is common-drain configured while the transconductor with a negative transconductance is common-source configured. All transistors are biased in the saturation. A notable advantage of the active inductor in Fig.2.27(b) is that all transistors are nMOS, making it attractive for high-frequency applications.

For Fig.2.27(a), we have $C_1 = C_{gs2}$, $G_{o1} \approx g_{o1}$, $G_{m1} = g_{m1}$, $C_2 = C_{gs1}$, $G_{o2} \approx g_{m1}$, and $G_{m2} = g_{m2}$, where g_{oj} and g_{mj}, $j = 1, 2$, are the output conductance and transconductance of transistor j, respectively. Using (2.9), we obtain the parameters of the equivalent RLC network of the active inductor

$$
\begin{aligned}
C_p &= C_{gs1}, \\
R_p &= \frac{1}{g_{m1}}, \\
L &= \frac{C_{gs2}}{g_{m1}g_{m2}}, \\
R_s &= \frac{g_{o1}}{g_{m1}g_{m2}}.
\end{aligned}
\tag{2.70}
$$

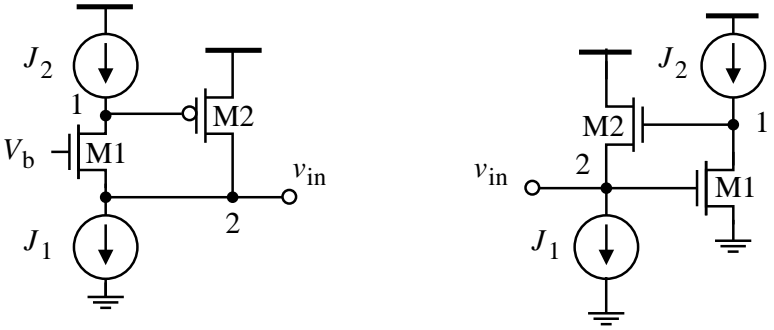


Figure 2.27. Simplified schematic of basic gyrator-C active inductors.

It is observed from (2.70) that the parasitic parallel resistance R_p is rather small, limiting the quality factor of the active inductor. Also, the parasitic series resistance is large, further lowering the quality factor. In evaluating the quality factor of this active inductor, the effect of the parasitic series resistance R_s is often neglected as R_p is small. In this case, the quality factor of the active inductor is obtained from

$$
Q \approx \frac{R_p}{\omega L} = \frac{\omega_{t2}}{\omega}. \tag{2.71}
$$

The self-resonant frequency of the active inductor is given by

$$
\omega_o \approx \frac{1}{\sqrt{LC_p}} = \sqrt{\omega_{t1}\omega_{t2}}, \tag{2.72}
$$

where

$$\omega_{tj} = \frac{g_{mj}}{C_{gsj}}, i = 1, 2 \tag{2.73}$$

is the cutoff frequency of transconductor j. At the self-resonance frequency of the active inductor $\omega_o = \sqrt{\omega_{t1}\omega_{t2}}$, the quality factor becomes

$$Q(\omega_o) = \sqrt{\frac{\omega_{t2}}{\omega_{t1}}}. \tag{2.74}$$

The frequency of the zero of the active inductor, which is the lower bound of the frequency range of the active inductor, is given by (2.18)

$$\omega_z = \frac{g_{o1}}{C_{gs2}}. \tag{2.75}$$

Eqs.(2.72) and (2.75) reveal that :

- In order to maximize the frequency range of the active inductor, ω_z should be minimized. This can be achieved by reducing g_{o1} or increasing C_{gs2}. The former is usually preferred as the latter lowers ω_o.
- Because the output impedance of deep sub-micron MOSFETs is small. The detrimental effect of $R_p = \frac{1}{g_{m1}}$ on the quality factor of the active inductor can not be neglected. The effect of R_p, however, can be eliminated by connecting a negative resistor of resistance $\hat{R}_p = -R_p$ in parallel with R_p.

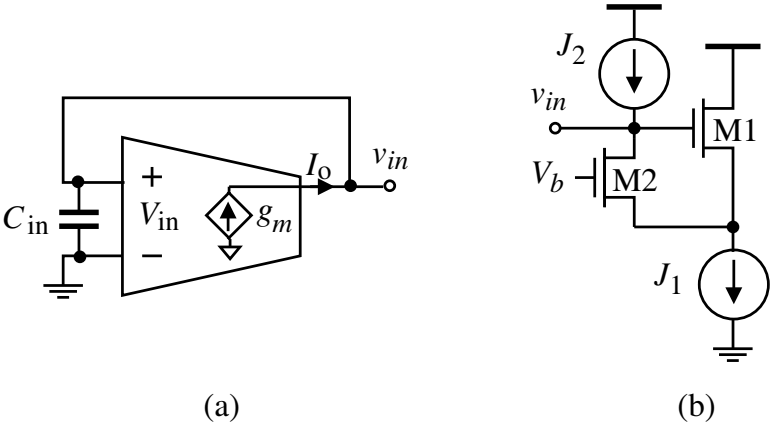


Figure 2.28. Single-ended negative impedance networks. (a) Block diagram. (b) Circuit implementation.

Negative resistors can be realized using transconductors with positive feedback, as shown in Fig.2.28 for single-ended negative resistors and Fig.2.29 for differential negative resistors. The positive feedback of the single-ended negative resistor in Fig.2.28 is depicted as the followings : An increase in the gate voltage of M_1 will increase the voltage at the source of M_1. Since M2 is a common-gate configuration, an increase in the source voltage of M2 will increase the drain voltage of M2. A positive feedback is thus established. Readers can verify the positive feedback of the differential negative resistors of Fig.2.29 in a similar manner. For Fig.2.29. It can be shown that the impedance at low frequencies is given by

$$Z \approx -\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right). \tag{2.76}$$

To maximize the frequency range over which a constant negative resistance exists, transconductors synthesizing negative resistors should be configured as simple as possible.

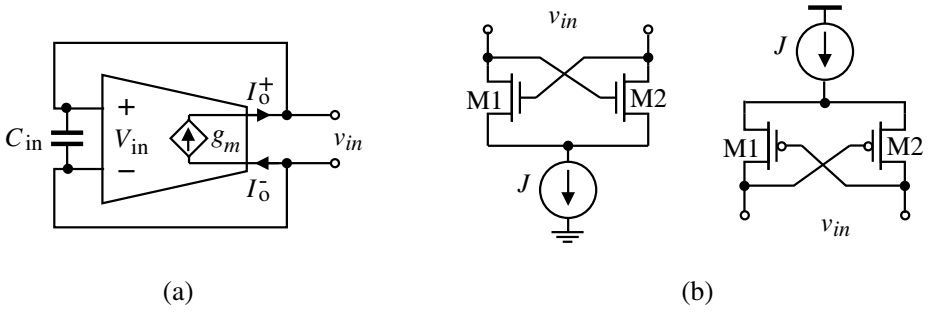


Figure 2.29. Differential negative impedance networks. (a) Block diagram. (b) Circuit implementation. The tail current source in the differential configuration can be removed, provided that biasing currents are provided by the circuit connected to the negative resistor. Note that the removal of the biasing tail current source will also remove the tunability of the resistance of the negative resistor.

- The effect of R_s can be compensated for in three different ways :
  - Use cascodes and regulated cascodes to reduce g_{o1} [37, 38, 65, 73]. It is well known that cascodes and regulated cascodes are effective means to boost the output impedance of transconductors. The price paid, however, is the reduced signal swing.
  - The reason that the preceding basic active inductors have a low R_p is because the input impedance of the positive transistor in Fig.2.27(a)

is $1/g_{m1}$ and the output impedance of the positive transconductor in Fig.2.27(b) is $1/g_{m2}$. The use of transconductors that have both a large output impedance and a large input impedance will eliminate this drawback. As an example, the differentially-configured positive transconductor of Karsilayan-Schaumann active inductors shown in Fig.2.16(b,c) has an infinite input impedance and a large output impedance r_{o2} [74, 75, 48, 49, 61].

– Because the series RL branch of the RLC equivalent network of the active inductor can be replaced with a parallel $\hat{R}\hat{L}$ branch. The inductance of the parallel $\hat{R}\hat{L}$ branch is given by $\hat{L} = L\Big(1 + \dfrac{1}{Q^2}\Big)$ while the resistance is given by $\hat{R}_p = (1 + Q^2)R_s$. The total parasitic parallel resistance of the active inductor becomes $R_{p,total} = R_p||\hat{R}_p$. The quality factor of the active inductor can be made infinite theoretically by employing a shunt negative resistor whose resistance is $-R_{p,total}$.

Table 2.3 compares the range of the voltage swing and the minimum supply voltage of the two basic active inductors. It is seen that the active inductor in Fig.2.27(a) offers a large input voltage swing and requires a lower minimum supply voltage.

Table 2.3. Comparison of the input voltage swing and the minimum supply voltage of the basic active inductors in Fig.2.27.

Active inductor	Fig.2.27(a)	Fig.2.27(b)
Max. input voltage	$V_{DD} - V_T - V_{sat}$	$V_{DD} - V_T - V_{sat}$
Min. input voltage	V_{sat}	V_T
Min. V_{DD}	$V_T + 2V_{sat}$	$2V_T + V_{sat}$

2.3.2 Wu Current-Reuse Active Inductors

Fig.2.30 show the schematic of Wu current-reuse active inductors proposed in [42, 45, 36]. In the nMOS version of the active inductor, the positive transconductor is common-gate configured while the negative transconductor is common-source configured. When only C_{gs} is considered, $C_1 = C_{gs2}$, $G_{o1} \approx g_{o1} + g_{o2}$, $G_{m1} = g_{m1}$, $C_2 = C_{gs1}$, $G_{o2} = \dfrac{1}{g_{m1}}$, and $G_{m2} = g_{m2}$. The parameters of the equivalent RLC network of this active inductor are given by

$$
\begin{aligned}
C_p &= C_{gs1}, \\
R_p &= \frac{1}{g_{m1}}, \\
L &= \frac{C_{gs2}}{g_{m1}g_{m2}}, \\
R_s &= \frac{g_{o1}+g_{o2}}{g_{m1}g_{m2}}.
\end{aligned}
\tag{2.77}
$$

The quality factor of Wu active inductors can be estimated by neglecting the effect of R_s and only focusing on R_p as R_p is small.

$$
Q \approx \frac{R_p}{\omega L} = \frac{\omega_{t2}}{\omega}. \tag{2.78}
$$

At the self-resonant frequency $\omega_o = \sqrt{\omega_{t1}\omega_{t2}}$, we have

$$
Q(\omega_o) \approx \sqrt{\frac{\omega_{t2}}{\omega_{t1}}}. \tag{2.79}
$$

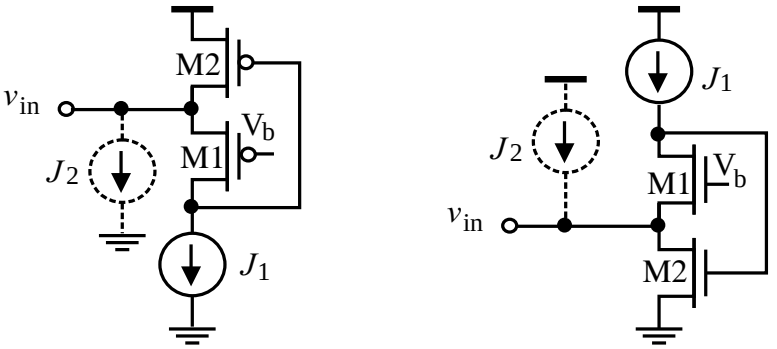


Figure 2.30. Simplified schematic of Wu current reuse active inductors.

It is seen from the preceding analysis that to increase ω_o, both ω_{t1} and ω_{t2} need to be increased. Increasing ω_{t1}, however, lowers $Q(\omega_o)$. Increasing ω_{t1} should therefore be avoided. To boost ω_{t2} without increasing ω_{t1}, the dc biasing current of M_1 is kept unchanged while that of M_2 is increased by injecting an additional current J_2 into M_2. The additional current source J_2 is used to boost the transconductance of M_2 such that the upper frequency bound can be increased without lowering the quality factor. In practical design, J_2 is

provided by the stage preceding to the inductors and the active inductors are known as Wu current-reuse active inductors.

2.3.3 Lin-Payne Active Inductors

The Lin-Payne active inductor proposed in [39] and shown in Fig.2.31 requires the minimum supply voltage of only $V_T + 2V_{sat}$. Another implementation of Lin-Payne active inductors is shown in Fig.2.32 [76]. The minimum supply voltage of the active inductor is also $V_T + 2V_{sat}$. They can be analyzed in a similar way as Wu current re-use active inductors.

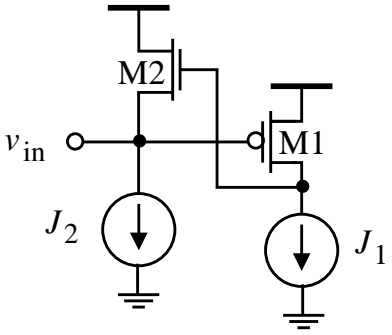


Figure 2.31. Simplified schematic of Lin-Payne active inductor.

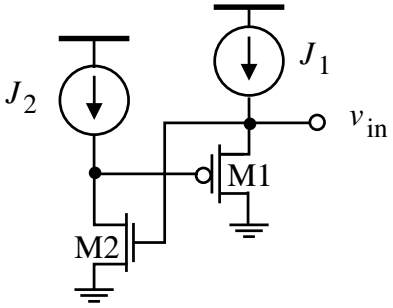


Figure 2.32. Simplified schematic of the variation of Lin-Payne active inductor.

2.3.4 Ngow-Thanachayanont Active Inductors

Ngow and Thanachayanont proposed the low-voltage active inductor shown in Fig.2.33[76]. The addition of M_3 branch relaxes the biasing difficulties encountered in Lin-Payne active inductors. M_{1-3} can easily be biased in the saturation to ensure a stable operation of the active inductors. The analysis of Ngow-Thanachayanont active inductors is similar to that of Wu current re-use active inductors and is left as an exercise for readers.

2.3.5 Hara Active Inductors

Although the MESFET implementation of Hara active inductors appeared two decades ago [77, 78], the CMOS version of Hara active inductors only emerged a few years ago [41, 40, 79–82]. Hara active inductors shown in Fig.2.34 employ only a MOSFET and a resistor. They are indeed gyrator-C active inductors. The feedback operation of nMOS Hara active inductor is as the followings : An increase of the input current will result in an increase in the voltage at the input node. Since the gate voltage is kept at V_{DD}, v_{GS} is reduced. This in turn lowers the current flowing out of the active inductor.

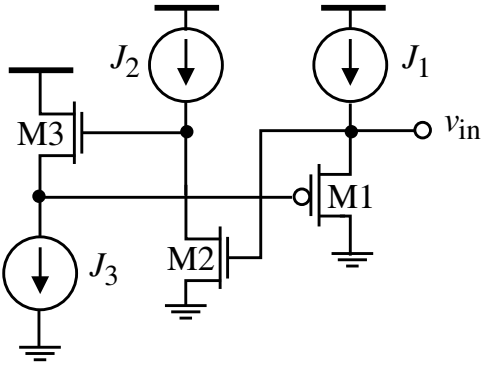
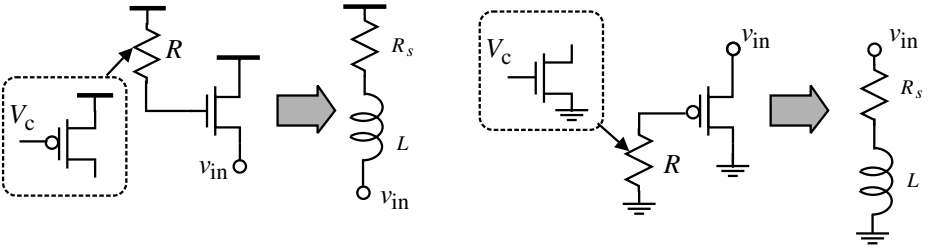


Figure 2.33. Simplified schematic of low-voltage gyrator-C active inductor.



(a) nMOS (b) pMOS

Figure 2.34. Hara active inductors. Resistor R can be made variable by implementing it using MOSFETs biased in the triode.

The input impedance of the nMOS Hara active inductor can be derived from its small-signal equivalent circuit shown in Fig.2.35

$$Z \approx \left(\frac{1}{RC_{gs}C_{gd}}\right)\frac{sRC_{gd}+1}{s^2+s\dfrac{g_m}{C_{gs}}+\dfrac{g_m}{RC_{gs}C_{gd}}}, \tag{2.80}$$

where $g_m \gg g_o$ and $C_{gs} \gg C_{gd}$ were utilized to simplify the results.

The self-resonant frequency ω_o and the frequency of the zero ω_z of the active inductor are given by

$$\begin{aligned} \omega_o &= \sqrt{\frac{g_m}{RC_{gs}C_{gd}}} = \sqrt{\omega_t \omega_z}, \\ \omega_z &= \frac{1}{RC_{gd}}, \end{aligned} \tag{2.81}$$

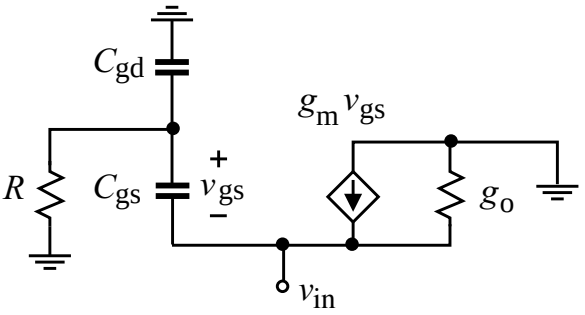


Figure 2.35. Small-signal equivalent circuit of nMOS Hara active inductors.

where

$$\omega_t = \frac{g_m}{C_{gs}}. \tag{2.82}$$

The Bodé plots of Hara active inductors are the same as those given in Fig.2.6. The network exhibits an inductive characteristic in the frequency range $\omega_z < \omega < \omega_o$. When C_{gd}, C_{sb}, C_{sb}, and high-order effects are neglected, the inductance L and parasitic series resistance R_s of nMOS Hara active inductors are given by

$$R_s = \frac{g_m + \omega^2 C_{gs}^2 R}{g_m^2 + \omega^2 C_{gs}^2}, \tag{2.83}$$

and

$$L = \frac{C_{gs}(g_m R - 1)}{g_m^2 + \omega^2 C_{gs}^2}. \tag{2.84}$$

Observe that

$$g_m R > 1 \tag{2.85}$$

is required to ensure $L > 0$. Under the condition $g_m R \gg 1$, Eqs.(2.83) and (2.84) can be written as

$$R_s = \frac{\frac{1}{g_m} + \left(\frac{\omega}{\omega_t}\right)^2 R}{1 + \left(\frac{\omega}{\omega_t}\right)^2} \approx \frac{1}{g_m}, \tag{2.86}$$

and

$$L = \frac{R}{\omega_t\left[1 + \left(\frac{\omega}{\omega_t}\right)^2\right]} \approx \frac{R}{\omega_t}, \tag{2.87}$$

where we have utilized $\left(\frac{\omega}{\omega_t}\right)^2 \approx 0$. It is evident from (2.87) that the inductance L is directly proportional to R and can be tuned by varying R. The series resistance R_s is largely dominated by g_m at frequencies below the cut-off frequency of the transistor.

The dependence of the input impedance of the nMOS Hara active inductor on the resistance of the resistor R and the width of the transistor is shown in Fig.2.36 and Fig.2.37, respectively. The active inductor was implemented in TSMC-0.18μm 1.8V CMOS technology and analyzed using SpectreRF with BSIM3V3 device models. It is observed that an increase of R will lower both ω_z and ω_o. This agrees with the theoretical results. Increasing the width of the transistor will lower ω_o because

$$\omega_t = \frac{g_m}{C_{gs}} \approx \frac{3}{2}\frac{\mu_n}{L_c^2}(V_{GS} - V_T), \tag{2.88}$$

where μ_n is the surface mobility of free electrons and L_c is the channel length, is independent of the width of the transistor. Also, L is nearly independent of g_m.

Hara active inductors suffer from the loss of the voltage headroom of at least V_T. In [41], a voltage doubler was used to increase the supply voltage for R. A drawback of this approach is the complexity of the voltage doubler and the need for a control clock.

2.3.6 Wu Folded Active Inductors

The drawback of Hara active inductors can be eliminated by employing Wu folded active inductors shown in Fig.2.38[83]. Wu folded active inductors were initially proposed by Thanachayanont in [84].

To derive the parameters of the RLC equivalent circuit of Wu folded active inductors, consider the nMOS version of Wu folded active inductors with its small-signal equivalent circuit shown in Fig.2.39. To simplify analysis, we neglect C_{gd}, g_o and other parasitic capacitances of the transistor. It can be shown that the input impedance is given by

$$Z = \frac{sRC_{gs} + 1}{sC_{gs} + g_m}. \tag{2.89}$$

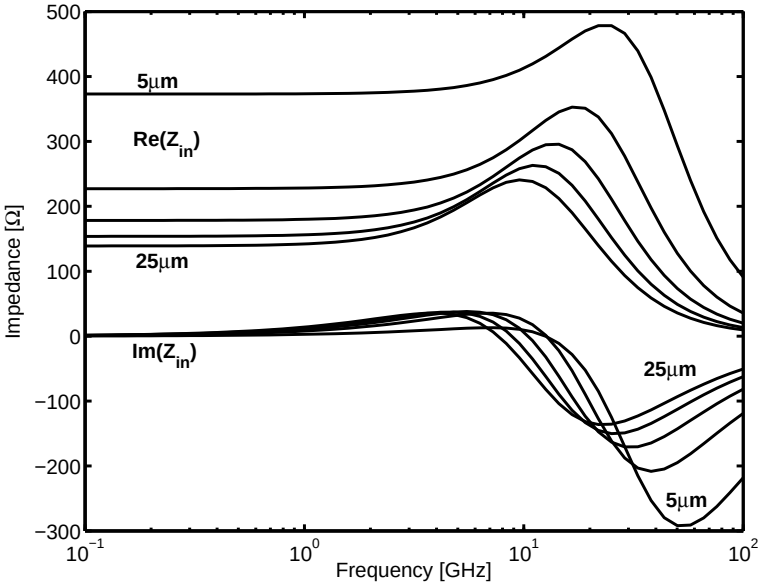


Figure 2.36. Dependence of Z of nMOS Hara active inductors on the width of the transistor. W is varied from 5μm to 25μm with step 5μm, $R = 1k\Omega$. DC biasing current 0.5mA.

It becomes evident that Z has a zero at frequency $\omega_z = \dfrac{1}{RC_{gs}}$ and a pole at frequency $\omega_p = \dfrac{g_m}{C_{gs}}$. The network is resistive at low frequencies $\omega < \omega_z$ with resistance $R \approx \dfrac{1}{g_m}$ and inductive when $\omega_z < \omega < \omega_p$. Note the behavior of the network beyond ω_p can not be quantified by (2.89) due to the omission of C_{gd}.

To derive its RLC equivalent circuit, we examine the input admittance of the network

$$\begin{aligned} Y_{in} &= \frac{sC_{gs} + g_m}{sRC_{gs} + 1} \\ &= \frac{1}{R} + \frac{1}{s\dfrac{RC_{gs}}{g_m - \frac{1}{R}} + \dfrac{1}{g_m - \frac{1}{R}}}. \end{aligned} \tag{2.90}$$

Eq.(2.90) can be represented by a series RL network in parallel with a resistor R_p with

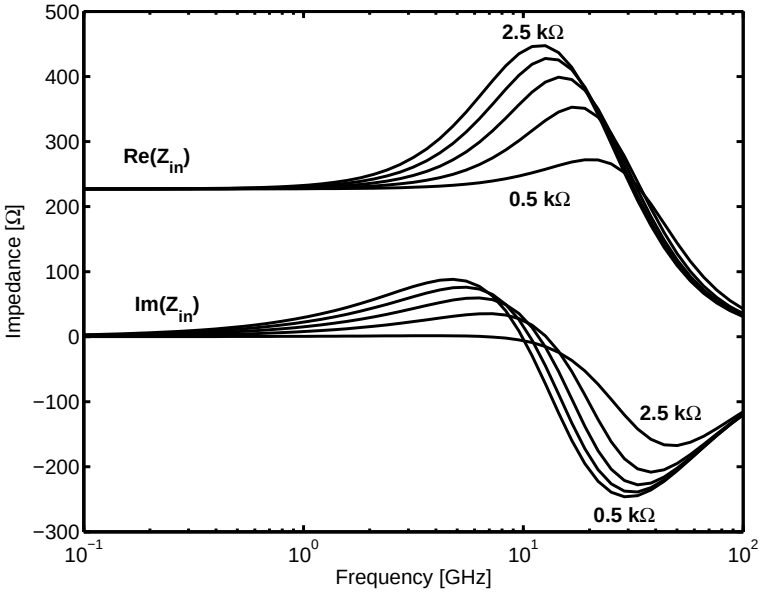


Figure 2.37. Dependence of Z of nMOS Hara active inductors on R. R is varied from 0.5 kΩ to 2.5 kΩ with step 0.5 kΩ, $W = 10\mu$m. DC biasing current 0.5mA.

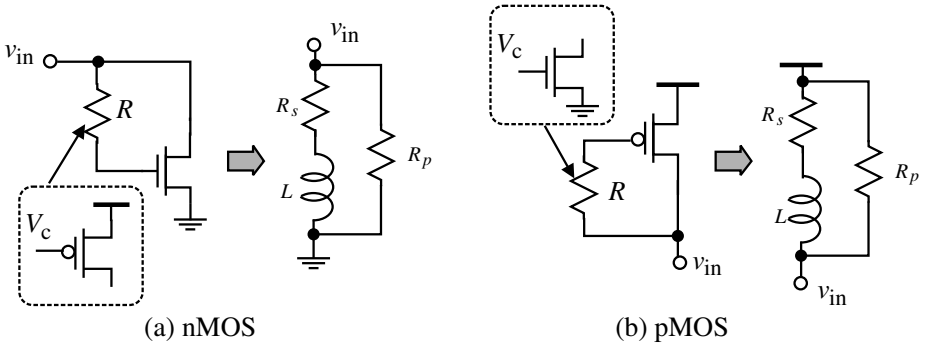


Figure 2.38. Simplified schematic of Wu folded active inductors.

$$
\begin{aligned}
R_p &= R, \\
L &= \frac{RC_{gs}}{g_m - \frac{1}{R}}, \\
R_s &= \frac{1}{g_m - \frac{1}{R}}.
\end{aligned}
\tag{2.91}
$$

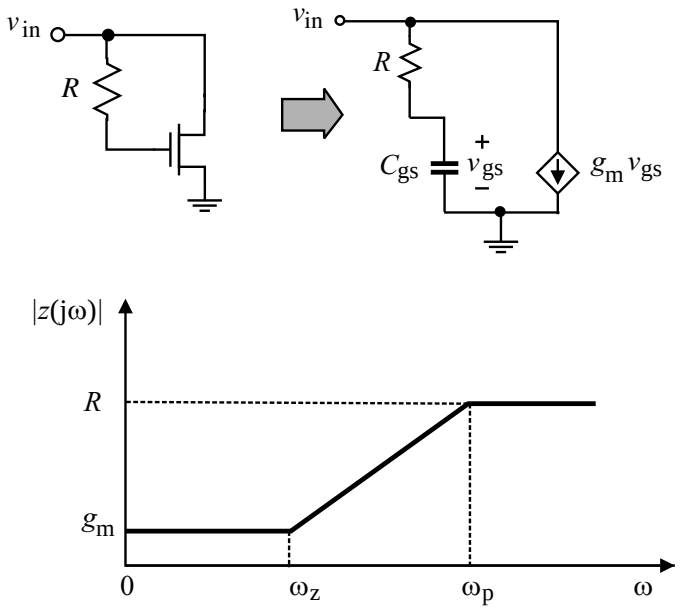


Figure 2.39. Small-signal equivalent circuit of the nMOS version of Wu folded active inductors.

It becomes evident that $g_m > \frac{1}{R}$ is required in order to have $L, R_s > 0$. Also, if $g_m \gg \frac{1}{R}$, we have $R_s \approx \frac{1}{g_m}$ and $L \approx \frac{RC_{gs}}{g_m} = \frac{R}{\omega_t}$. They are the same as those of the corresponding Hara active inductor investigated earlier.

2.3.7 Karsilayan-Schaumann Active Inductors

The active inductor proposed by Karsilayan and Schaumann is shown in Fig.2.40 [74, 75, 48, 49, 61]. It was also developed by Yodprasit and Ngarmnil in [85]. The active inductor consists of a differentially configured transconductor with a positive transconductance and a common-source transconductor with a negative transconductance.

A. Lossless Karsilayan-Schaumann Active Inductors

The inductance of the inductor can be derived from the small-signal analysis of the inductor with the assumption $g_{ds} = 0$. The admittance of the active inductor is given by

$$Y = sC_{gs1}\frac{sC_{gs2} + g_{m2}}{s(C_{gs1} + C_{gs2}) + (g_{m1} + g_{m2})}$$

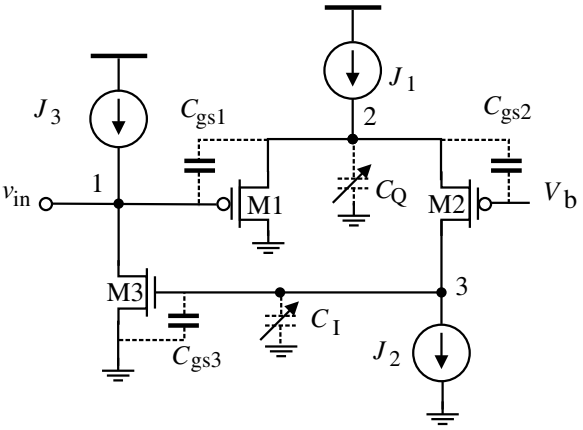


Figure 2.40. Simplified schematic of Karsilayan-Schaumann active inductor.

$$+ \quad \frac{g_{m2}g_{m3}}{sC_{gs3}} \frac{sC_{gs1} + g_{m1}}{s(C_{gs1} + C_{gs2}) + (g_{m1} + g_{m2})}. \tag{2.92}$$

Further assume M_1 and M_2 are perfectly matched, i.e. $g_{m1} = g_{m2} = g_m$ and $C_{gs1} = C_{gs2} = C_{gs}$. Eq.(2.92) is simplified to

$$Y = \frac{1}{s\left(\frac{2C_{gs3}}{g_m g_{m3}}\right)} + s\left(\frac{C_{gs}}{2}\right). \tag{2.93}$$

Eq.(2.93) reveals that the active inductor can be represented by a capacitor in parallel with an inductor. The capacitance and inductance are given by

$$\begin{aligned} C_p &= \frac{C_{gs}}{2}, \\ L &= \frac{2C_{gs3}}{g_m g_{m3}}. \end{aligned} \tag{2.94}$$

It is interesting to note that the preceding results can also be obtained using the results given in (2.9) directly. The differentially-configured transconductor with only one of its two input terminals is connected to the input has a transconductance $\frac{g_m}{2}$. The capacitance encountered at the input node of the active inductor is given by $\frac{C_{gs}}{2}$ as capacitors of C_{gs1} and C_{gs2} are connected in series.

Eq.(2.94) reveals that the inductance of the active inductor can be increased by increasing the capacitance between the gate and source of M_3. This can be

achieved by adding an auxiliary capacitor C_I in parallel with C_{gs3}, as shown in Fig.2.40. The inductance in this case becomes

$$L = \frac{2(C_{gs3} + C_I)}{g_m g_{m3}}. \tag{2.95}$$

The auxiliary capacitor C_I can be implemented using MOS varactors. The inductance of the active inductor can be tuned in this way.

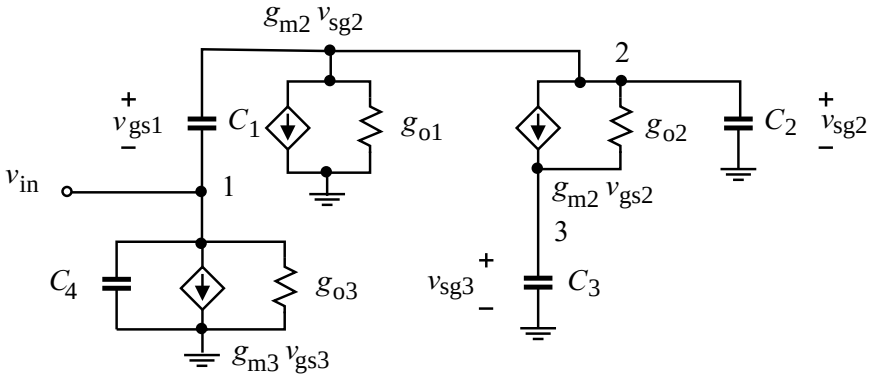


Figure 2.41. Small-signal equivalent circuit of Karsilayan-Schaumann active inductor.

B. Lossy Karsilayan-Schaumann Active Inductors

The preceding analysis excludes the effect of g_{ds} and other parasitic capacitances of the transistors. Due to the absence of the lossy conductance g_{ds}, the quality factor of the active inductor can not be studied. In what follows, we investigate the quality factor of the active inductor and its tunability by following the approach of Karsilayan and Schaumann. The small-signal equivalent circuit of the active inductor is shown in Fig.2.41 where C_1, C_2, C_3, and C_4 represent the total capacitances including both intrinsic and parasitic capacitances encountered at or between respective nodes. It was shown in [74] that the admittance of the active inductor is given by

$$Y \approx \frac{1}{j\omega\Big(\dfrac{2C_3}{g_m g_{m3}}\Big) + \dfrac{G(\omega)}{g_m g_{m3}}}, \tag{2.96}$$

where

$$G(\omega) = g_{o2} + 2g_{o4} - \omega^2 C_3\Big(\frac{C_1 + C_2}{g_m}\Big). \tag{2.97}$$

The active inductor can be represented by an inductor of inductance

$$L = \frac{2C_3}{g_m g_{m3}} \tag{2.98}$$

in series with a resistor of resistance

$$R_s = \frac{G(\omega)}{g_m g_{m3}}. \tag{2.99}$$

The quality factor of the active inductor is obtained from

$$Q \approx \frac{\omega L}{R_s} = \frac{2\omega C_3}{G(\omega)}. \tag{2.100}$$

It is observed from (2.100) that if we set $G(\omega) = 0$, i.e.

$$C_2 = \frac{(g_{o2} + 2g_{o4})g_m}{\omega^2 C_3} - C_1, \tag{2.101}$$

the quality factor of the active inductor will become infinite. To achieve this, an auxiliary capacitor C_Q can be added at the source of M_1 and M_2, as shown in Fig.2.40. An important observation is that Q is tuned by varying C_Q, which is the capacitance encountered at the source of M_1 and M_3 while the inductance of the active inductor is tuned by varying C_I, the capacitance of the auxiliary capacitor added between the gate and source of M_3. In other words, Q and L can be tuned independently.

It was demonstrated in [74] that the quality factor of the active inductor was made nearly 400 and the inductance of the active inductor exceeded 600 nH in a 0.5μm CMOS implementation of Karsilayan-Schaumann active inductor.

C. Variations of Karsilayan-Schaumann Active Inductors

To increase the speed of the active inductor and to reduce the silicon consumption, it was shown by Xiao and Schaumann in [61] that the preceding Karsilayan-Schaumann active inductor can also be implemented using all nMOS transistors (excluding biasing current sources), as shown in Fig.2.42. Implemented in TSMC-0.18μm CMOS technology, this active inductor exhibited a self-resonant frequency of 6.68 GHz and a quality factor of 106.

In [86, 87], the common-source configured transconductor of the preceding Karsilayan-Schaumann active inductor was replaced with a static inverter to boost the transconductance of the transconductor from g_{m3} to $g_{m3} + g_{m4}$, as shown in Fig.2.43. The inductance is tuned by varying C_Q while the quality

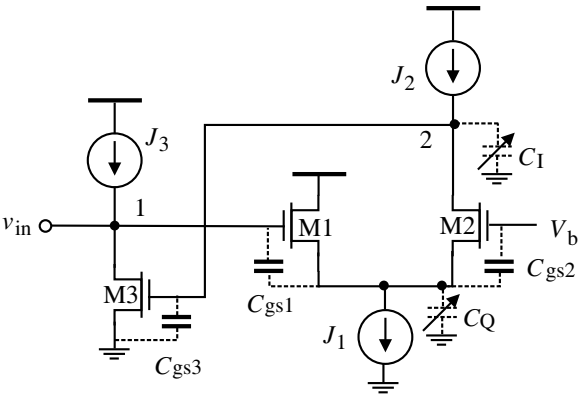


Figure 2.42. Simplified schematic of Karsilayan-Schaumann active inductor using nMOS transistors only.

factor is tuned by changing C_I. The input voltage of the static inverter must satisfy $V_{IL} \leq v_2 \leq V_{IH}$ where V_{IL} and V_{IH} are the lower and upper voltage bounds of the transition region of the static inverter, respectively, in order to ensure that M_3 and M_4 are in the saturation. A disadvantage of this design is the stringent constraint imposed on the voltage swing of node 2 of the active inductor.

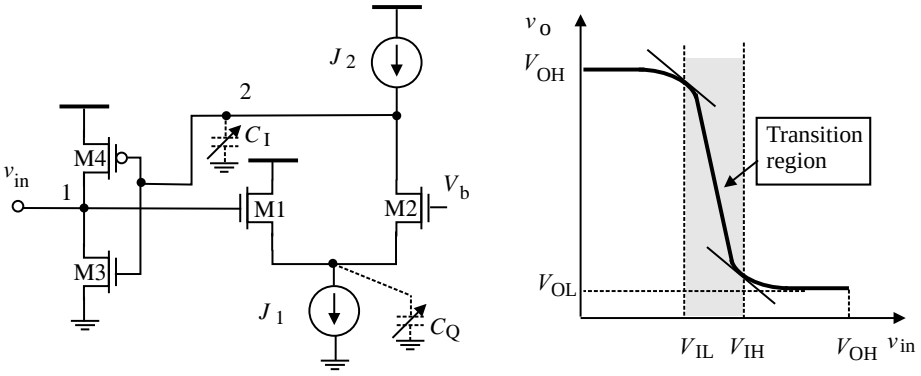


Figure 2.43. Simplified schematic of Karsilayan-Schaumann active inductor using a static-inverter negative transconductor.

2.3.8 Yodprasit-Ngarmnil Active Inductors

It was pointed out earlier that to boost the quality factor, the effect of both R_s and R_p of an active inductor must be compensated for. The $L \sim R_s$ series branch of the RLC equivalent circuit of an active inductor can be replaced with

the $L \sim \hat{R}_p$ parallel branch shown in Fig.2.44(b) with the inductance and the shunt resistance given by

$$\begin{aligned} \hat{L} &= L(1 + \frac{1}{Q^2}), \\ \hat{R}_p &= R_p(1 + Q^2). \end{aligned} \tag{2.102}$$

Both $\hat{R}_p$ and R_p can be combined into a single parallel resistor of resistance $R_{p,total} = \hat{R}_p || R_p$.

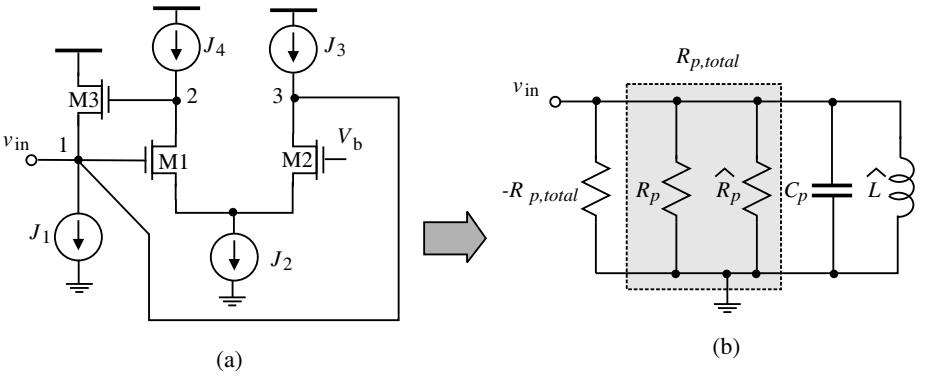


Figure 2.44. Simplified schematic of Yodprasit-Ngarmnil active inductor.

To boost the quality factor, a negative resistor of resistance $-R_{p,total}$ can be connected in parallel with $R_{p,total}$, as shown in Fig.2.44(b), such that the net resistive loss of the active inductor vanishes. It was also shown earlier that negative resistors are realized by using positive feedback. In Fig.2.44(a), the added electrical connection between the input terminal of the active inductor and the drain of M_2 forms the needed positive feedback. This is because an increase in v_{in} will result in an increase in i_{D1}, subsequently a decrease in i_{D2} as $i_{D1} + i_{D2} = J_2$ (constant). This is echoed with an increase in the drain voltage of M_2, which will further increase v_{in}. The impedance looking into the gate of M_1 at low frequencies is given by

$$Z_{in} \approx -\Big(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\Big). \tag{2.103}$$

The preceding analysis reveals that the differential pair offers two distinct functions simultaneously :

- It behaves as a transconductor with a negative transconductance to construct the gyrator-C active inductor.
- It provides the needed negative resistance between the input terminal and the ground to cancel out the parasitic resistances of the active inductor.

When g_o is considered, it was shown in [85] that the quality factor of Yodprasit-Ngarmnil active inductor is given by

$$Q = \frac{\sqrt{g_{m3}g_{m1}C_{gs3}C_{gs1}}}{\frac{C_{gs1}}{r_{o1}} + \frac{2C_{gs3}}{r_{o3}}}. \tag{2.104}$$

Eq.(2.104) shows that Q can be tuned by either changing $g_{m1,2}$ or $r_{o1,2}$. Because the former also changes the inductance of the inductor, the preferred choice is therefore to vary r_o of M_1 and M_2, which can be achieved by employing the cascode configuration of the differential-pair transconductor and varying the gate voltage of M_4 and M_5, as shown in Fig.2.45. r_{o1} and r_{o2} in Fig.2.45 now become $(g_{m4}r_{o4})r_{o1}$ and $(g_{m5}r_{o5})r_{o2}$, respectively. Transconductances $g_{m4,5}$ can be tuned by varying the gate voltage of $M_{4,5}$. As demonstrated in [85], Q was tuned up to 12000 in a 0.6μm implementation of the active inductor.

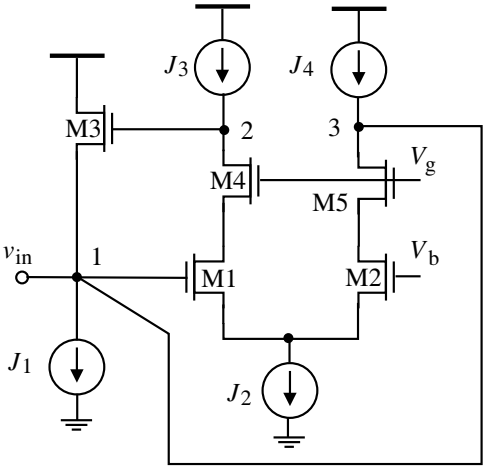


Figure 2.45. Simplified schematic of Cascode Yodprasit-Ngarmnil active inductors.

2.3.9 Uyanik-Tarim Active Inductor

The CMOS active inductor proposed by Uyanik and Tarim in [88] with its simplified schematic shown in Fig.2.46 only has two transistors connected in

series between V_{DD} and ground rails, making it very attractive for low-voltage applications. As seen in Fig.2.46, M_1 and J form a transconductor with a negative transconductance g_{m1}. $M_{2,3,4}$ form a transconductor with a positive transconductance $\frac{g_{m2}g_{m4}}{g_{m3}} = g_{m2}$, provided that M_3 and M_4 are identical. To tune the inductance of the active inductor without affecting the parasitic series resistance of the active inductor, which controls the quality factor of the active inductor, a varactor C is added between the gate of M_2 and the ground.

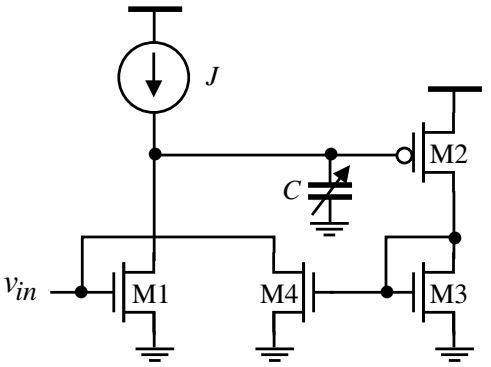


Figure 2.46. Simplified schematic of Uyanik-Tarim active inductor.

Implemented in UMC-0.13μm 1.2V CMOS technology, the simulation results in [88] shows that the active inductor had a wide frequency range from 0.3 GHz to its self-resonant frequency of approximately 7.32 GHz. The quality factor of the active inductor exceeded 100 in the frequency range 4.8-6.4 GHz with its phase error less than 1 degree. The maximum quality factor was 3900, occurring at 5.75 GHz. The minimum number of transistors stacked between the power and ground rails also enabled the active inductor to have a large input signal swing of 18 mV. The inductance was from 38 nH to 144 nH.

2.3.10 Carreto-Castro Active Inductors

The BiCMOS active inductors proposed by Carreto-Castro in [89] can also be implemented in CMOS technologies, as shown in Fig.2.47. Neglecting C_{gd} and g_o of the transistor. The input impedance of nMOS Carreto-Castro active inductor is given by

$$Z = \frac{1}{g_m}\frac{sRC_{gs}+1}{s\frac{C_{gs}}{g_m}+1}. \tag{2.105}$$

The zero of $Z(s)$ is at frequency

$$\omega_z = \frac{1}{RC_{gs}} \tag{2.106}$$

and the pole of $Z(s)$ is at frequency

$$\omega_p = \frac{g_m}{C_{gs}}. \tag{2.107}$$

The inductance of Carreto-Castro active inductor can be derived by examining the input admittance

$$\begin{aligned} Y &= \frac{sC + g_m}{sRC + 1} \\ &= \frac{1}{R} + \frac{1}{s\left(\dfrac{RC}{g_m - \frac{1}{R}}\right) + \dfrac{1}{g_m - \frac{1}{R}}}. \end{aligned} \tag{2.108}$$

It is seen from (2.108) that the parameters of the RLC equivalent circuit of the active inductor are given by

$$\begin{aligned} R_p &= R, \\ L &= \frac{R^2 C}{Rg_m - 1}, \\ R_s &= \frac{R}{Rg_m - 1}. \end{aligned} \tag{2.109}$$

In order to have $L > 0$ and $R_s > 0$,

$$Rg_m > 1 \tag{2.110}$$

is required. This condition also ensures that $\omega_z < \omega_p$. In the frequency range $\omega_z < \omega < \omega_p$, the circuit is inductive. Because

$$\frac{\omega_p}{\omega_z} = Rg_m, \tag{2.111}$$

for practical applications, $Rg_m \gg 1$ is usually required to maximize the effective frequency range. In this case

$$L \approx \frac{RC}{g_m} = \frac{R}{\omega_t},$$
$$R_s \approx \frac{1}{g_m}. \tag{2.112}$$

It is interesting to note that Hara active inductors, Wu folded active inductors, and Carreto-Castro active inductors all have the same expressions for L and R_s.

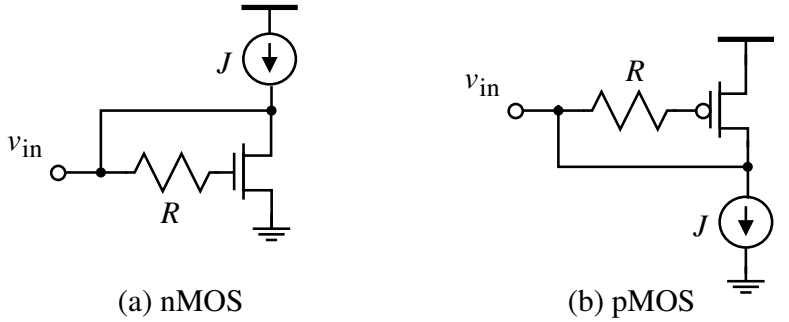


Figure 2.47. Simplified schematic of Carreto-Castro active inductors.

Figs.2.48 and 2.49 show the dependence of the resistance and reactance of a nMOS Carreto-Castro active inductor on R and J. The active inductor was implemented in TSMC-0.18μm 1.8V CMOS technology and analyzed using SpectreRF with BSIM3V3 device models.

2.3.11 Thanachayanont-Payne Cascode Active Inductors

It was pointed out earlier that to maximize the frequency range of active inductors, ω_z should be minimized and ω_o should be maximized. Maximizing ω_o is rather difficult because ω_o of active inductors is set by the cut-off frequency of the transconductors constituting the active inductors. The frequency of the zero of active inductors given by $\omega_z = \dfrac{g_{o1}}{C_{gs2}}$, on the other hand, can be lowered by either increasing C_{gs2} or decreasing g_{o1}. The former is at the cost of lowering ω_o and should therefore be avoided. To reduce g_{o1}, Thanachayanont and Payne proposed the cascode active inductors shown in Fig.2.50 [90, 65, 73]. Cascode can be implemented in either of the two transconductors, as shown in Fig.2.50. Note that a modification in the polarity of the transconductors is required to ensure the existence of a negative feedback in the gyrator-C configuration.

The impedance of Thanachayanont-Payne cascode active inductor is given by

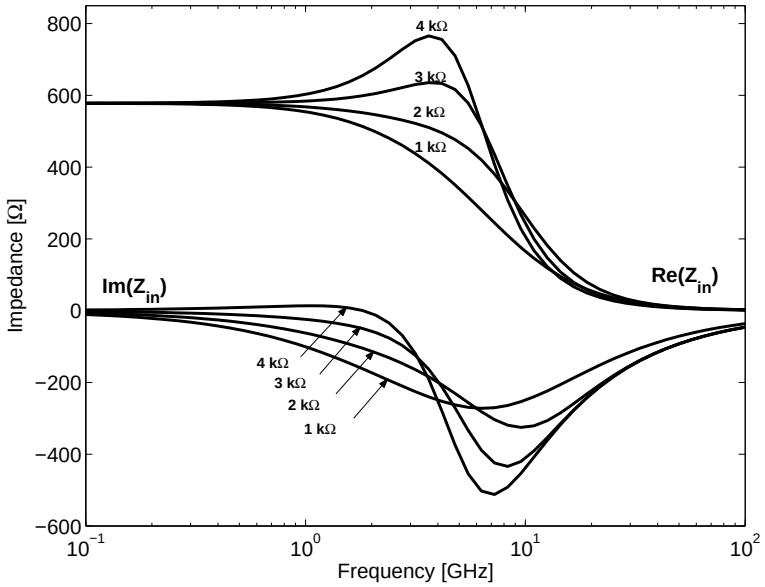


Figure 2.48. Dependence of Z of nMOS Carreto-Castro active inductor on R. Circuit parameters : $L = 0.18\mu$m, $W = 10\mu$m, $R = 2k\Omega$.

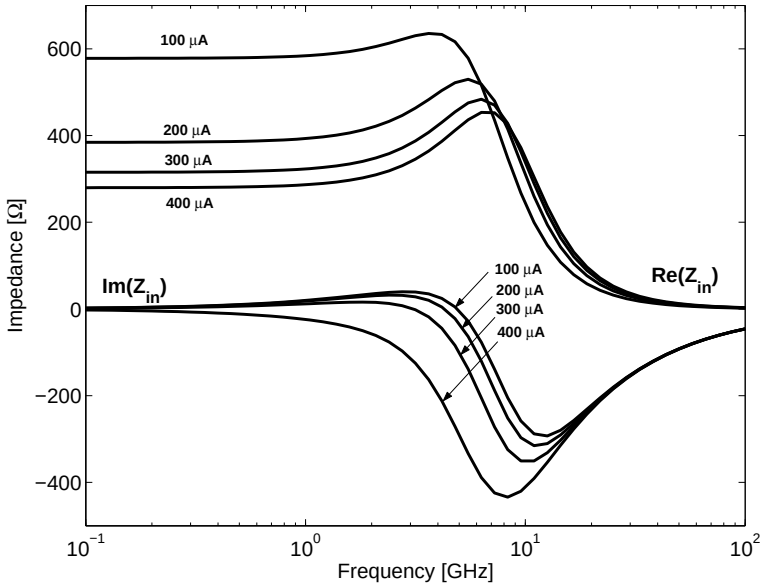


Figure 2.49. Dependence of Z of nMOS Carreto-Castro active inductor on J. Circuit parameters : $L = 0.18\mu$m, $W = 10\mu$m, $R = 2k\Omega$.

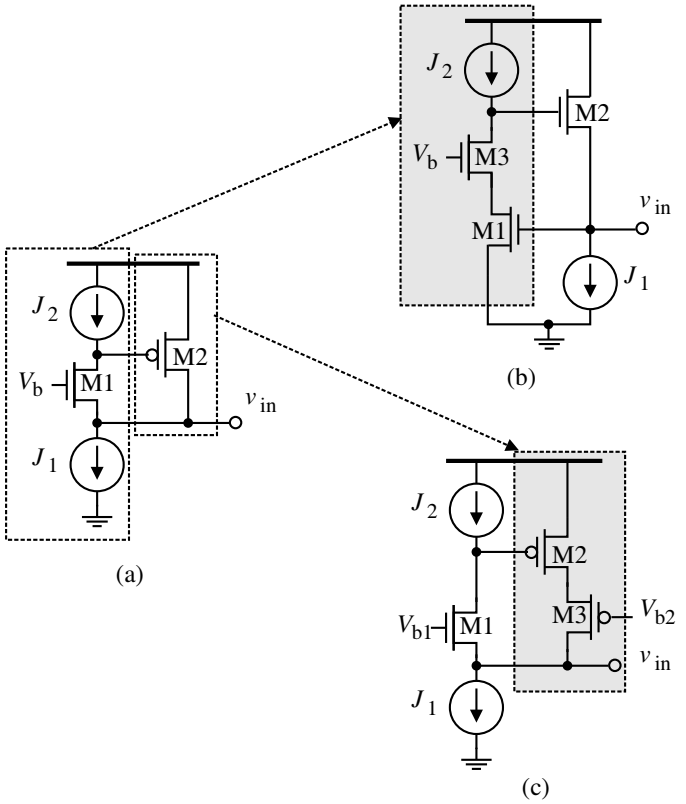


Figure 2.50. Simplified schematic of Thanachayanont-Payne cascode active inductors. (a) Basic active inductor. (b,c) Thanachayanont-Payne cascode active inductors.

$$Z \approx \left(\frac{g_{o1} g_{o3}}{C_{gs1} C_{gs2} g_{m3}} \right) \frac{s \left(\dfrac{C_{gs2} g_{m3}}{g_{o1} g_{o3}} \right) + 1}{s^2 + s \left(\dfrac{g_{o1} g_{o3}}{C_{gs2} g_{m3}} + \dfrac{g_{o1}}{C_{gs1}} \right) + \dfrac{g_{m1} g_{m2}}{C_{gs1} C_{gs2}}}, \qquad (2.113)$$

where $g_m \gg g_o$ was utilized in simplifying the results. It is seen from (2.113) that the frequency of the zero of Z is reduced from

$$\omega_z = \frac{g_{o1}}{C_{gs2}} \qquad (2.114)$$

without the cascode to

$$\omega_z = \left(\frac{g_{o1}}{C_{gs2}}\right)\frac{1}{g_{m3}r_{o3}} \tag{2.115}$$

with the cascode. The self-resonant frequency of the active inductor given by

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} = \sqrt{\omega_{t1}\omega_{t2}}, \tag{2.116}$$

however, remains unchanged. It should not be surprised to see that cascodes do not change ω_o. This is because cascodes are not subject to Miller effect and has no effect on the bandwidth. Cascode configurations thus can effectively expend the frequency range of active inductors by lowering the lower bound of the frequency range of active inductors.

The parameters of the RLC equivalent network of the cascode active inductor can be obtained by examining the admittance of the cascode inductor and the results are given by

$$\begin{aligned} R_p &= \frac{1}{g_{o2}}, \\ C_p &= C_{gs1}, \\ R_s &= \left(\frac{g_{o1}}{g_{m1}g_{m2}}\right)\frac{1}{g_{m3}r_{o3}}, \\ L &= \frac{C_{gs2}}{g_{m1}g_{m2}}. \end{aligned} \tag{2.117}$$

It is evident from (2.117) that the cascode active inductor has the same inductance as that of the corresponding non-cascode gyrator-C active inductor. The parasitic series resistance is reduced from

$$R_s = \frac{g_{o1}}{g_{m1}g_{m2}} \tag{2.118}$$

without the cascode to

$$R_s = \frac{g_{o1}}{g_{m1}g_{m2}}\left(\frac{1}{g_{m3}r_{o3}}\right) \tag{2.119}$$

with the cascode. The parallel resistance is increased from

$$R_p = \frac{1}{g_{m1}} \tag{2.120}$$

without the cascode to

$$R_p = \frac{1}{g_{o2}}. \tag{2.121}$$

with the cascode. Both improve the quality factor of the active inductor, as is evident from

$$Q \approx \frac{\omega L}{R_s} = \omega C_{gs2} r_{o1} \quad (R_s \text{ dominates}) \tag{2.122}$$

or

$$Q \approx \frac{R_p}{\omega L} = \frac{g_{m2}}{\omega C_{gs2}} \quad (R_p \text{ dominates}) \tag{2.123}$$

without the cascode and

$$Q \approx \frac{\omega L}{R_s} = \omega C_{gs2} r_{o1} (g_{m3} r_{o3}) \quad (R_s \text{ dominates}) \tag{2.124}$$

or

$$Q \approx \frac{R_p}{\omega L} = (r_{o2} g_{m1}) \frac{g_{m2}}{\omega C_{gs2}} \quad (R_p \text{ dominates}) \tag{2.125}$$

with the cascode. To summarize, the cascode configurations of gyrator-C active inductors offer the following attractive characteristics :

- Frequency range expansion by lowering the lower bound of the frequency range.
- Quality factor improvement by lowering the parasitic series resistance R_s and increasing the parasitic parallel resistance R_p.
- No reduction in the upper bound of the frequency range.
- No reduction in the inductance.
- The minimum supply voltage of the active inductor without the cascode is given by $V_T + 2V_{sat}$. For the cascode active inductor of Fig.2.50(b), $V_{DD,min} = 2V_T + V_{sat}$. For the cascode active inductor of Fig.2.50(c), $V_{DD,min} = V_T + 2V_{sat}$.

2.3.12 Weng-Kuo Cascode Active Inductors

Weng and Kuo proposed a current-reuse cascode active inductor in [62] to eliminate the drawback of the preceding Thanachayanont-Payne cascode active inductors that the inductance and quality factor can not be tuned independently. The simplified schematic of Weng-Kuo active inductor is shown in Fig.2.51. It is seen that g_{m1} is proportional to $J_1 + J_3$ while g_{m3} is only proportional to J_1. Because $L = \dfrac{C_{gs2}}{g_{m1}g_{m2}}$, $R_s = \dfrac{g_{o1}g_{o3}}{g_{m1}g_{m2}g_{m3}}$, $C_p = C_{gs1}$, and $R_p = \dfrac{1}{g_{o2}}$, we have

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}},$$
$$Q(\omega_o) = \frac{\omega_o L}{R_s} = \frac{g_{m3}}{g_{o1}g_{o3}}\sqrt{\frac{g_{m1}g_{m2}C_{gs2}}{C_{gs1}}}. \tag{2.126}$$

ω_o can be tuned by varying g_{m1} and g_{m2} while Q can be tuned by varying g_{m3} only. So the tuning of Q can be made independent of ω_o. Note that because the tuning of ω_o, however, will affect Q, an adjustment of Q is therefore required after each tuning of ω_o.

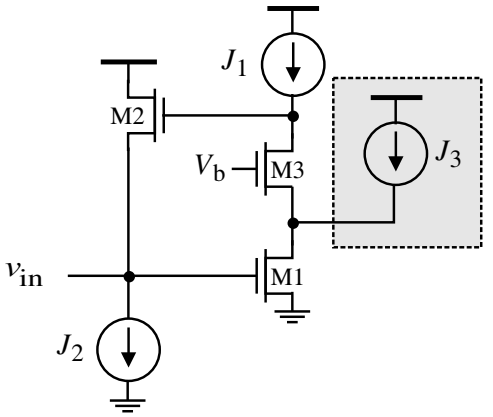


Figure 2.51. Simplified schematic of Weng-Kuo active inductor.

2.3.13 Manetakis Regulated Cascode Active Inductors

The performance of the preceding cascode active inductors can be improved by further reducing R_s. This is achieved by using regulated cascodes and multi-regulated cascodes, as shown in Fig.2.52 [91]. The parameters of the

RLC equivalent circuit of the regulated cascode gyrator-C active inductor are given by

$$\begin{aligned} G_{o1} &= \frac{1}{g_{o1}(r_{o3}g_{m3})(r_{o4}g_{m4})}, \\ C_1 &= C_{gs2}, \\ G_{o2} &= g_{o2}, \\ C_2 &= C_{gs1}, \end{aligned} \tag{2.127}$$

from which we obtain

$$\begin{aligned} R_p &= \frac{1}{G_{o2}}, \\ C_p &= C_2, \\ R_s &= \frac{G_{o1}}{g_{m1}g_{m2}}, \\ L &= \frac{C_1}{g_{m1}g_{m2}}. \end{aligned} \tag{2.128}$$

Because $\omega_z = \dfrac{G_{o1}}{C_1}$ and $\omega_o = \dfrac{1}{\sqrt{LC_p}}$, the lower bound of the frequency is reduced while the upper bound of the frequency range remains unchanged.

The parameters of the RLC equivalent circuit of the multi-regulated cascode gyrator-C active inductor are given by

$$\begin{aligned} G_{o1} &= \frac{1}{g_{o1}(r_{o3}g_{m3})(r_{o4}g_{m4})(r_{o5}g_{m5})}, \\ C_1 &= C_{gs2}, \\ G_{o2} &= g_{o2}, \\ C_2 &= C_{gs1}. \end{aligned} \tag{2.129}$$

It is evident from (2.129) that the lower bound of the frequency is further reduced while the upper bound of the frequency range remains unchanged.

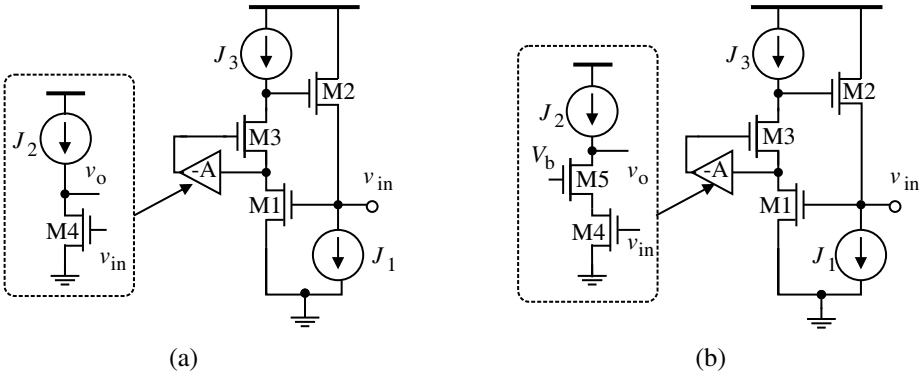


Figure 2.52. Simplified schematic of Manetakis regulated and multi-regulated cascode active inductors. (a) Regulated cascode active inductors. (b) Multi-regulated cascode active inductors.

The simulation results of cascode active inductors, regulated cascode active inductors and multi-regulated cascode active inductors given in [91] demonstrated that regulated cascode reduced the lower frequency bound of active inductors by one decade while multi-regulated cascode further reduced the lower frequency bond by more than one decade.

2.3.14 Hsiao Feedback Resistance Cascode Active Inductors

It was shown earlier that cascode active inductors offer a large frequency range and a high quality factor. To further improve the quality factor, feedback resistance active inductors shown in Fig.2.53 were proposed by Hsiao *et al.* in [92]. This type of active inductors was further investigated in [93, 94]. By assuming that the biasing current source transistors M_n and M_p are ideal, the parameters of the RLC equivalent circuit of the active inductor are given by

$$
\begin{aligned}
C_p &= C_{gs3}, \\
R_p &= \frac{R_f g_{o2} + 1}{2g_{o2} + R_f g_{o2}^2}, \\
R_s &= \frac{g_{m1} g_{o2} g_{o3} + \omega^2 [g_{m2} C_{gs1}^2 - g_{m1} C_{gs1} C_{gs2} (R_f g_{o2} + 1)]}{g_{m1}^2 g_{m2} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2}, \\
L &= \frac{g_{m1} g_{m2} C_{gs1} + \omega^2 C_{gs1}^2 C_{gs2} (R_f g_{o2} + 1)}{g_{m1}^2 g_{m2} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2}.
\end{aligned}
\tag{2.130}
$$

It is seen from (2.130) that the added feedback resistor R_f lowers R_s and increases L simultaneously. Both boost the quality factor of the active inductor. The resistance of the feedback resistor R_f can be tuned by connecting a nMOS transistor in parallel with a poly resistor, as shown in the figure. Note R_f does not consume any static power. For the special case where $R_f = 0$, Eq.(2.130) becomes

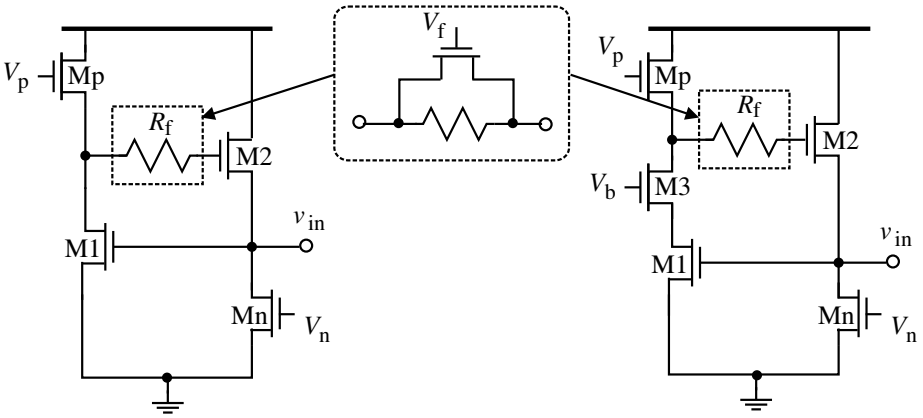
$$\begin{aligned} C_p &= C_{gs3}, \\ R_p &\approx \frac{1}{g_{o2}}, \\ R_s &\approx \frac{g_{o2}g_{o3}}{g_{m1}g_{m2}g_{m3}}, \\ L &= \frac{C_{gs2}}{g_{m1}g_{m2}}. \end{aligned} \tag{2.131}$$

It should be noted that the self-resonant frequency of the active inductor with the feedback resistors R_f is reduced due to the increase of L. It was shown in [94] that the decrease of the self-resonant frequency of the feedback resistance active inductors can be compensated for by varying the biasing voltage V_p of the current-source transistor M_p. The simulation results of a feedback resistance active inductor implemented in a 0.18μm CMOS technology showed that the inductance of the inductor was 15 nH with the quality factor exceeding 50 and the self-resonant frequency of several GHz [92–94].

The preceding Hsiao feedback resistance cascode active inductors were further developed by Liang *et al.* where the cascode portion of the active inductor is replaced with a regulated cascode branch, as shown in Fig.2.54 so that the advantages of the regulated cascodes active inductor investigated earlier can be utilized [50].

2.3.15 Abdalla Feedback Resistance Active Inductors

Karsilayan-Schaumann active inductors studied earlier offer the key advantage of the independent tuning of their inductance and quality factor. In [95], Abdalla *et al.* modified Karsilayan-Schaumann active inductors by adding a feedback resistor between the two transconductors of the active inductor to improve the quality factor of the inductor, as shown in Fig.2.55. The added feedback resistor increases the inductance of the active inductor and at the same time lowers the parasitic series resistance of the active inductor, thereby boosting the quality factor of the active inductor. C_I and C_Q are MOS varactors to tune the inductance and quality factor of the active inductor, respectively.



(a) Feedback resistance active inductor

(b) Cascode feedback resistance active inductor

Figure 2.53. Simplified schematic of Hsiao feedback resistance active inductors.

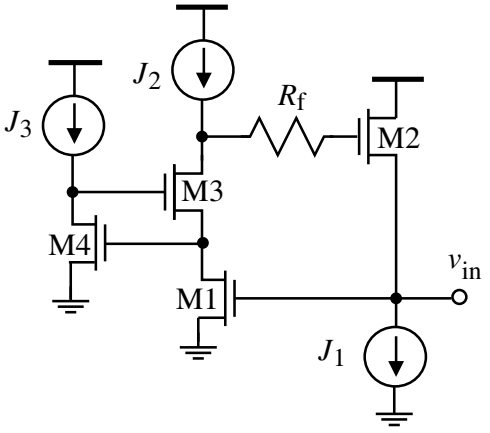


Figure 2.54. Simplified schematic of Liang feedback resistance regular cascode active inductors.

2.3.16 Nair Active Inductors

Wei *et al.* proposed a MESFET-version high-Q active inductor with loss compensated by a feedback network in [96]. This active inductor was modified and implemented in CMOS by Nair *et al.* in [97] and was used in design of a low-power low-noise amplifier for ultra wideband applications. The simplified schematic of Nair active inductor is shown in Fig.2.56. It is a cascode active inductor with a negative feedback network consisting of R_1, R_2, and C_2. It was shown in [97] that the parameters of this active inductor are given by

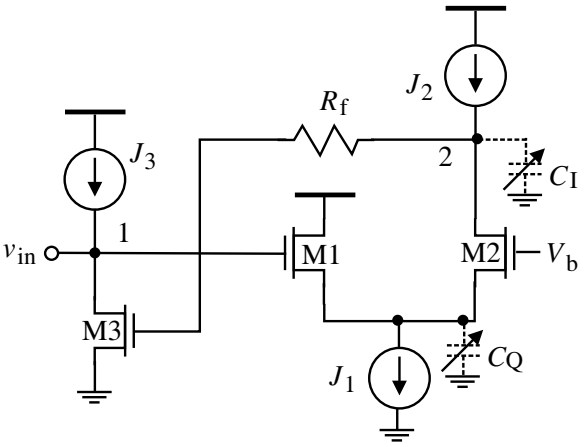


Figure 2.55. Simplified schematic of single-ended Abdalla feedback resistance active inductors.

$$L = \frac{C_3 + C_{gs3}}{g_{m1} g_{m3}},$$

$$\omega_o = \sqrt{\frac{g_{m1} g_{m3}}{C_{gs1}(C_3 + C_{gs3})}}, \tag{2.132}$$

$$Q(\omega_o) = \sqrt{\frac{g_{m1} g_{m3}(C_3 + C_{gs3})}{C_{gs1} g_{o1}^2}}.$$

It is seen from (2.132) that C_3 is used to boost the inductance. It also increases the quality factor and decreases the self-resonant frequency of the active inductor. The RC network consisting of $R_1, R_2 - C_2$ is a negative feedback network that reduces the parasitic resistances of the active inductor.

2.3.17 Active Inductors with Low Supply-Voltage Sensitivity

It was pointed out earlier that the parameters of gyrator-C active inductors, such as the inductance and parasitic resistances, are sensitive to the fluctuation of the supply voltage of the active inductors. This is because a V_{DD} fluctuation not only alters the dc operating point of the transconductors constituting the active inductors, it also changes the junction capacitances of the active inductors. Replica-biasing is an effective means to reduce the effect of supply voltage fluctuation on the inductance of active inductors. Fig.2.57 shows the configuration of Wu current-reuse active inductors with replica biasing [66]. The

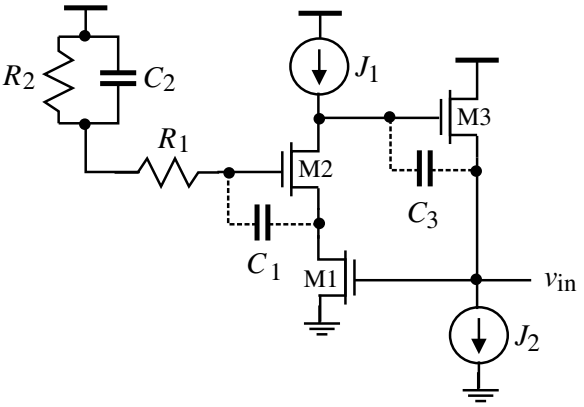


Figure 2.56. Simplified schematic of Nair active inductors.

replica-biasing section consists of a sensing circuit made of $M_{4,5,6}$ and an auxiliary voltage amplifier. An increase in V_{DD} will lead to an increase in $v_{SG3,6}$, subsequently the channel current of $M_{3,6}$. The voltage of the non-inverting terminal of the amplifier will also increase. The output of the amplifier will increase the gate voltage of $M_{3,6}$, which ensures that $v_{SG3,6}$ is kept unchanged approximately, minimizing the effect of V_{DD} fluctuation. The width of the transistors in the replica-biasing section should be the same as that of the active inductor section so that both will sense the same voltage change caused by the variation of V_{DD}.

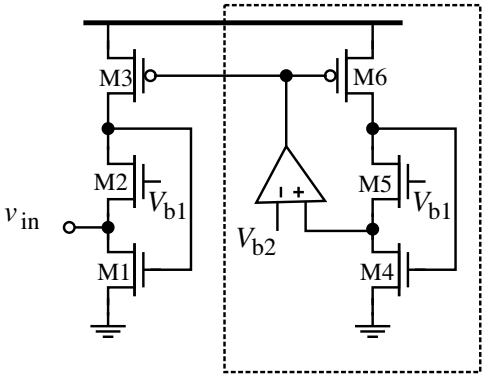


Figure 2.57. Simplified schematic of Wu current reuse active inductor (nMOS) with replica biasing.

2.4 Implementation of Differential Active Inductors

2.4.1 Lu Floating Active Inductors

The schematic of the active inductor proposed by Lu *et al.* is shown in Fig.2.58 [60]. It is a differentially configured gyrator-C active inductor. Transistors M_5 and M_6 are biased in the triode region and behave as voltage-controlled resistors whose resistances are controlled by the gate voltage V_b. All other transistors are biased in the saturation.

The negative feedback of the active inductor is as the followings : an increase in v_{1+} and a decrease in v_{1-} will result in an increase in v_{2+} and a decrease in v_{2-} due to the common-gate operation of $M_{1,2}$. The source followers of $M_{3,4}$ ensure that v_{1+} and v_{1-} will be reduced accordingly by approximately the same amount.

To find out the parameters of the RLC equivalent circuit of the active inductor, we represent M_5 and M_6 with channel conductances g_{ds5} and g_{ds6}, respectively, in the small-signal equivalent circuit of the active inductor. It can be shown that the differential input impedance of the inductor is given by

$$Z = \frac{2[s(C_{gs1} + C_{gs3}) - g_{m1} + g_{ds5}]}{g_{ds5}[g_{m1} + g_{m3} + s(C_{gs1} + C_{gs3})]}. \tag{2.133}$$

The parameters of the RLC equivalent circuit of the active inductor are given by

$$\begin{aligned} R_p &= \frac{2}{g_{ds5}}, \\ R_s &= \frac{2(g_{ds5} - g_{m1})}{g_{ds5}(2g_{m1} + g_{m3} - g_{ds5})}, \\ L &= \frac{2(C_{gs1} + C_{gs3})}{g_{ds5}(2g_{m1} + g_{m3} - g_{ds5})}. \end{aligned} \tag{2.134}$$

Note that $2g_{m1} + g_{m3} > g_{ds5}$ and $g_{ds5} > g_{m1}$ are required in order for R_s and L to have a positive value. The preceding development reveals that the inductance of the active inductor can be tuned by varying V_b, subsequently g_{ds5}. An increase in V_b will push M_5 and M_6 from the triode region towards the saturation region, lowering g_{ds5} and g_{ds6}. This is echoed with an increase in the inductance of the inductor.

2.4.2 Grözing Floating Active Inductors

As pointed out earlier that floating gyrator-C active inductors can be constructed using a pair of differential transconductors. One of the simplest differ-

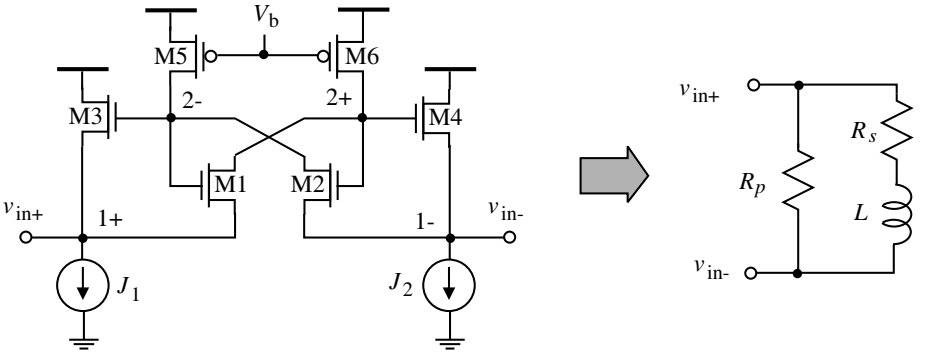


Figure 2.58. Simplified schematic of Lu floating active inductor.

entially configured transconductors is the basic differential pair. The floating active inductor proposed in [43, 44] and shown in Fig.2.59 employs two basic differential-pair transconductors. Two negative resistors are connected across the output nodes of the transconductors to cancel out the parasitic resistances of the active inductor. The inductance of the active inductor is tuned by varying the transconductances of the transconductors. This is done by adjusting the tail currents of the differential pairs $J_{1,2}$. The quality factor of the active inductor is tuned by varying the resistances of the negative resistors. This is attained by changing the tail current sources $J_{3,4}$ of the negative resistors. It was shown in [43, 44] that in a 0.18μm implementation of the active inductor, the quality factor of the active inductor was 600 at 2 GHz while the self-resonant frequency of the active inductor was 5.6 GHz

2.4.3 Thanachayanont Floating Active Inductors

The floating active inductor proposed in [37, 38, 98, 99, 65, 73] is shown in Fig.2.60. It consists of two cascode-configured gyrator-C active inductors investigated earlier. Transistors $M_{4,5}$ form a negative resistor to cancel out the parasitic resistances of the active inductor so as to boost its quality factor. Note that the resistance of the negative resistor can not be tuned in this implementation. The inductance of the active inductor is tuned by varying J_2. The active inductor implemented in a 0.35μm CMOS technology offered an inductance of 70 nH and a self-resonant frequency of 2.8 GHz. The quality factor exceeded 100 over the frequency range from 0.83 GHz to 1.33 GHz with its maxima of 1970 at 1.08 GHz.

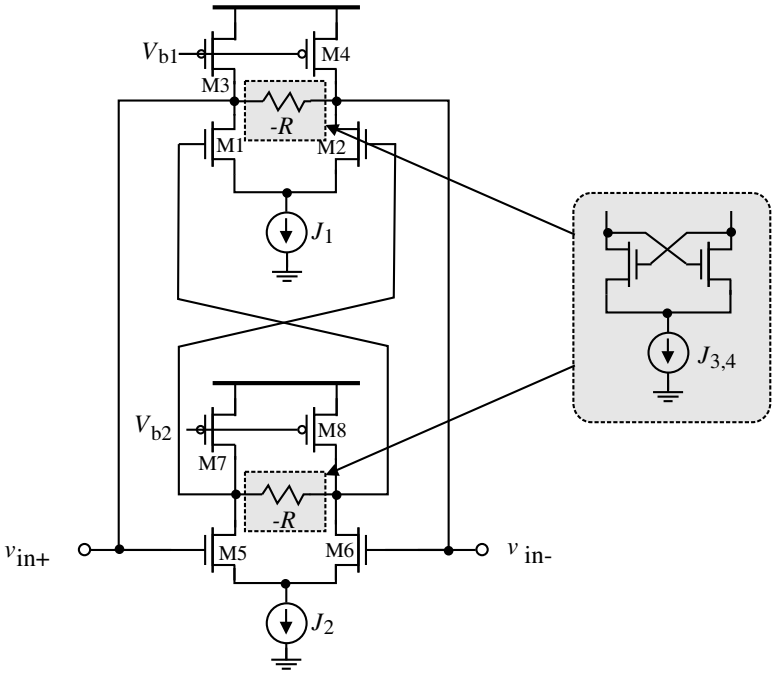


Figure 2.59. Simplified schematic of Grözing floating active inductor.

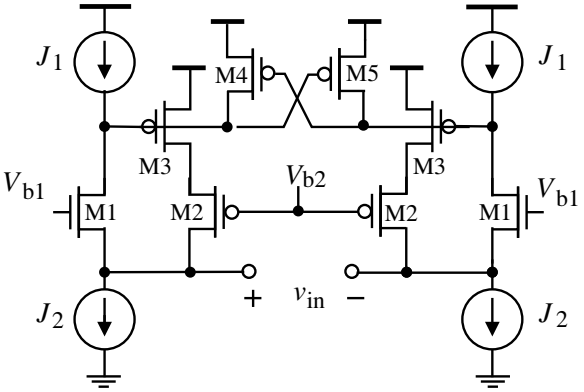


Figure 2.60. Simplified schematic of Thanachayanont floating active inductor.

2.4.4 Mahmoudi-Salama Floating Active Inductors

The floating active inductor proposed by Mahmoudi and Salama was used in the design of quadrature down converter for wireless applications [56, 100]. The schematic of Mahmoudi-Salama floating active inductor is shown in Fig.2.61. It consists of a pair of differential transconductors and a pair of negative resistors

at the output of the transconductors. $M_{8,16}$ are biased in the triode and behave as voltage-controlled resistors. They are added to the conventional cross-coupled configuration of negative resistors to provide the tunability of the resistance of the negative resistors without using a tail current source.

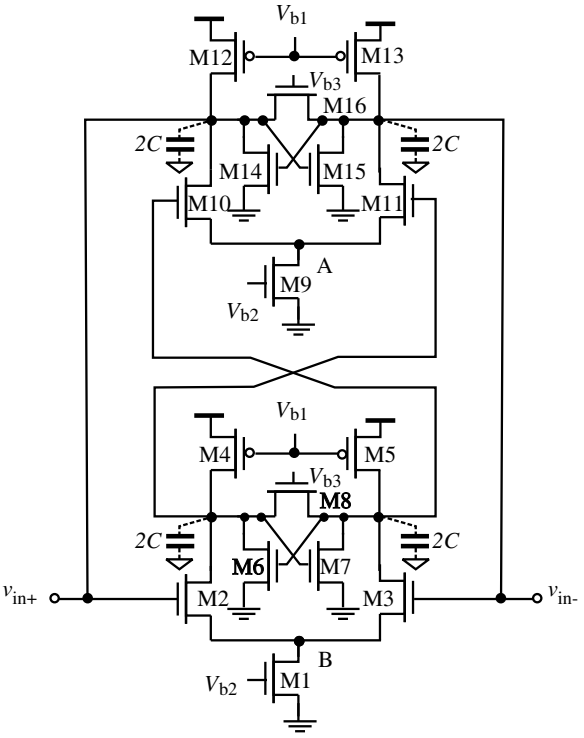


Figure 2.61. Simplified schematic of Mahmoudi-Salama floating active inductor.

The small-signal equivalent circuit of the tunable negative resistor is shown in Fig.2.62 where a test voltage source V_x is added for the derivation of the equivalent resistance of the negative resistor. R represents the resistance of M_8. Writing KCL at nodes 1 and 2 yields

$$\begin{aligned} g_{m1}V_2 + \frac{V_x}{R} - I_x = 0 \qquad & \text{(node 1)}, \\ g_{m1}(V_x + V_2) - \frac{V_x}{R} + I_x = 0 \quad & \text{(node 2)}. \end{aligned} \tag{2.135}$$

The resistance of the negative resistors at low frequencies is obtained from (2.135)

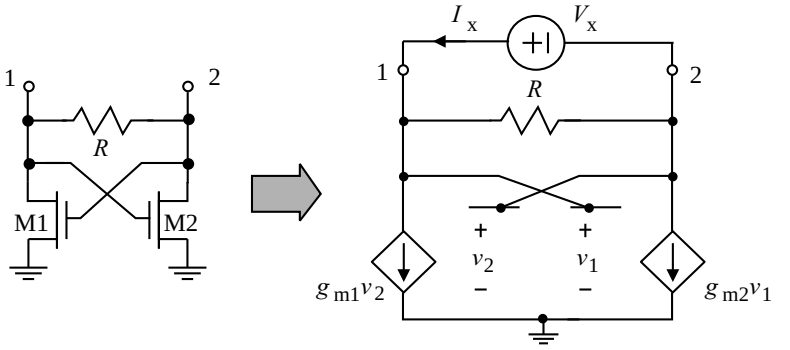


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Figure 2.62. Small-signal equivalent circuit of Mahmoudi-Salama floating active inductor at low frequencies. g_o of the transistors is neglected.

$$\begin{aligned} Z &= \frac{V_x}{I_x} = -\frac{R\Big(\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\Big)}{R-\Big(\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\Big)} \\ &= R//\Bigg[-\Big(\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\Big)\Bigg]. \end{aligned} \tag{2.136}$$

The inductance of the active inductor is given by $L = \dfrac{C}{G_{m1}G_{m2}}$, where $2C$ is the total capacitance encountered at each of the output nodes of the transconductor, G_{m1} and G_{m2} are the transconductances of the differential transconductors 1 and 2, respectively. By assuming that nodes A and B are the virtual ground and neglecting C_{gd} and the diffusion junction capacitances, we have $C \approx \dfrac{C_{gs2,3,10,11}}{2}$ and $G_m = g_{m2,3,10,11}$.

2.4.5 Feedback Resistance Floating Active Inductors

The feedback resistance technique studied earlier was also employed in the design of floating active inductors by Akbari-Dilmaghani *et al.* in [101] to improve the performance of these inductors. A similar approach was used by Abdalla *et al.* in design of high-frequency phase shifters [102]. This section investigates these active inductors.

The schematic of the feedback resistance floating active inductor proposed by Akbari-Dilmaghani *et al.* is shown in Fig.2.63. It consists of two basic differential-pair transconductors and two feedback resistors. The functionality of the added feedback resistors is the same as that of the single-ended active

inductors investigated earlier, i.e. lowering the parasitic series resistance and increasing the inductance.

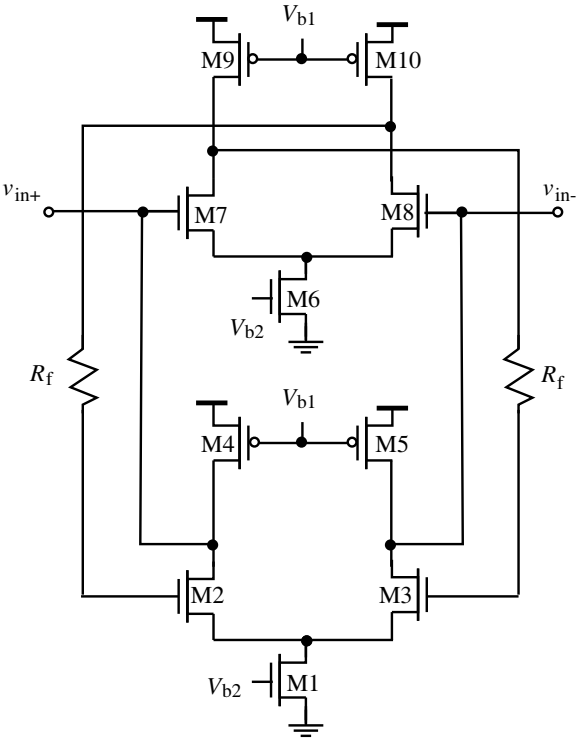


Figure 2.63. Simplified schematic of Akbari-Dilmaghani feedback resistance floating active inductor.

The simplified schematic of Abdalla differential feedback resistance floating active inductors is shown in Fig.2.64, $M_{11,12}$ are biased in the triode and behave as voltage-controlled resistors. It was shown in [102] that the inductance and the parasitic series resistance of the floating active inductor are given by

$$\begin{aligned} L &= \frac{C + C_{gs4,5}\left(1 + \dfrac{R_f}{R_T}\right)}{g_{m1,2}g_{m4,5}}, \\ R_s &= \frac{\dfrac{1}{R_T} - \omega^2 C_{gs4,5} C R_f}{g_{m1,2}g_{m4,5}}, \end{aligned} \tag{2.137}$$

where

$$C = C_{gd7,8} + C_{db1,2} + C_{db7,8} + C_{gs1,2},$$
$$R_T = R_f||R_{ds11,12}||r_{o1,2}||r_{o7,8}. \tag{2.138}$$

It is evident from (2.137) that R_f boosts L and lowers R_s simultaneously. Both improve the performance of the floating active inductor. Also seen from (2.137) and (2.138) that $M_{11,12}$ control the series resistance R_s of the active inductor. By adjusting V_{b1}, R_s can be minimized.

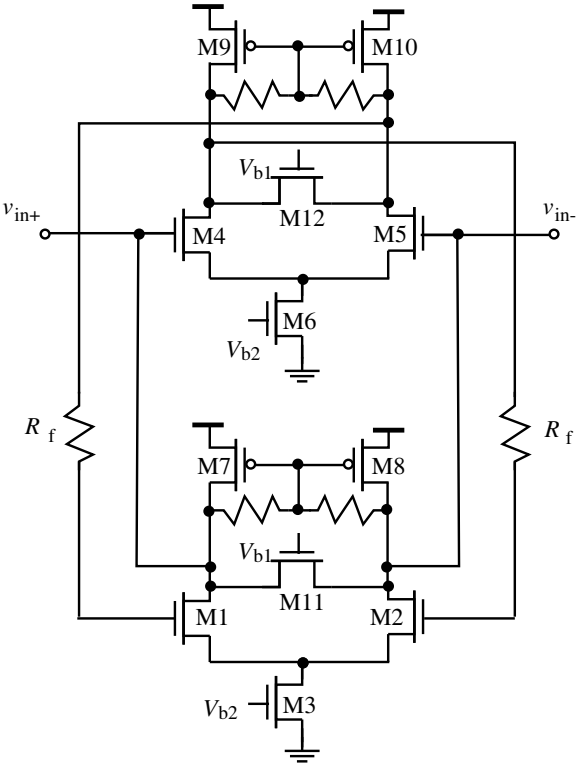


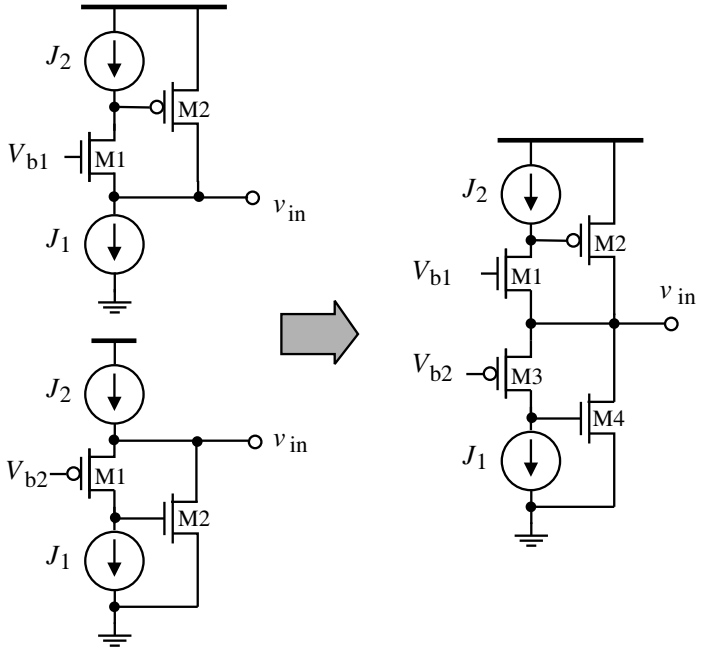
Figure 2.64. Simplified schematic differential Abdalla feedback resistance floating active inductors.

2.5 Class AB Active Inductors

The active inductors investigated up to this point fall into the category of class A active inductors. These class A active inductors suffer from a common drawback of a small voltage swing at the terminals of the active inductors, mainly due to the constraint that the input transistors of the transconductors of the active inductors should be biased and operated in the saturation. Note that

although the input transistors of the transconductors of active inductors can be pushed into the triode region while still exhibiting an inductive characteristic, the nonlinearity of the active inductors will increase.

To increase the voltage swing of the active inductors without sacrificing linearity, class AB configurations can be employed. A class AB active inductor can be constructed from a nMOS-configured class A active inductor and a pMOS-configured class A active inductor, as shown in Fig.2.65 [65]. When the input voltage is high, only the nMOS class A active inductor is activated. When the input voltage is low, only the pMOS class A active inductor is activated, i.e. the two active inductors are operated in an interleave manner, depending upon the swing of the input voltage. The network thus exhibits an inductive characteristic over a large input voltage range. The swing of the input voltage and the minimum supply voltage of the class A and class AB active inductors are compared in Table 2.4. It is seen that the need for a large minimum supply voltage of class AB active inductors makes them less attractive for low-voltage applications. It should also be noted that when $V_T + V_{sat} \leq v_{in} \leq V_{DD} - (V_T + V_{sat})$, both the nMOS and pMOS class A active inductors are activated.



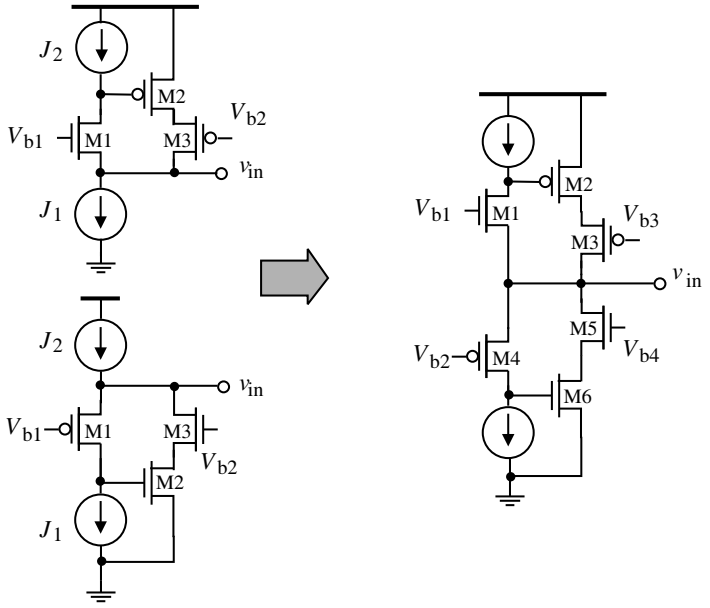
(a) Class A active inductors (b) Class AB active inductor

Figure 2.65. Simplified schematic of Thanachayanont-Ngow class AB active inductor.

Table 2.4. A comparison of the input voltage swing and the minimum supply voltage of class A and class AB active inductors.

	Class A (nMOS)	Class A (pMOS)	Class AB
$V_{in,min}$	V_{sat}	$V_T + V_{sat}$	0
$V_{in,max}$	$V_{DD} - (V_T + V_{sat})$	$V_{DD} - V_{sat}$	V_{DD}
$V_{DD,min}$	$V_T + 2V_{sat}$	$V_T + 2V_{sat}$	$2V_T + 2V_{sat}$

Class AB active inductors can also be configured in cascodes to increase the frequency range and to boost the quality factor, as shown in Fig.2.66. Floating cascode class AB active inductors can also be constructed in a similar manner as that of non-cascode floating active inductors, as shown in Fig.2.67. Negative resistance compensation techniques can be employed to improve the performance of class AB active inductors.



(a) Cascode class A active inductors (b) Cascode class AB active inductor

Figure 2.66. Simplified schematic of Thanachayanont-Ngow cascode class AB active inductor.

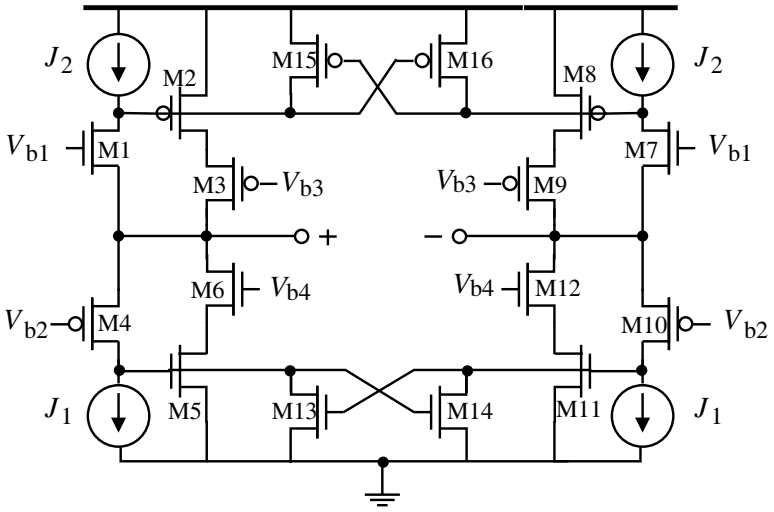


Figure 2.67. Simplified schematic of Thanachayanont-Ngow cascode floating class AB active inductors.

2.6 Chapter Summary

An in-depth examination of the principles, topologies, characteristics, and implementation of gyrator-C active inductors in CMOS technologies has been presented. We have shown that both single-ended and floating (differential) active inductors can be synthesized using gyrator-C networks. Lossless gyrator-C networks yield lossless active inductors while lossy gyrator-C networks synthesize lossy active inductors. To provide a quantitative measure of the performance of active inductors, a number of figure-of-merits have been introduced. These figure-of-merits include frequency range, inductance tunability, quality factor, noise, linearity, stability, supply voltage sensitivity, parameter sensitivity, signal sensitivity, and power consumption. Frequency range specifies the lower and upper bounds of the frequency in which gyrator-C networks are inductive. We have shown that the low frequency bound is set by the frequency of the zero of the gyrator-C networks while the upper frequency bound is set by the frequency of the pole of the networks. Both are due to the finite input and output impedances of the transconductors constituting active inductors. One of the key advantages of active inductors over their spiral counterparts is the large tunability of their inductance. We have shown that the inductance of gyrator-C active inductors can be tuned by varying either the transconductances of the transconductors or the load capacitance. The former is often used for the coarse control of the inductance whereas the latter is used for the fine control of the inductance. The distinct sensitivities of the quality factor of active inductors to their parasitic series and parallel resistances have been investigated. We have

shown that the parasitic series resistance of an active inductor can be converted to an equivalent parallel parasitic resistance such that a negative shunt resistor can be employed to cancel out the effect of both the series and parallel parasitic resistances of the active inductor simultaneously. An emphasis has been given to the noise of active inductors as these inductors exhibit a high level of noise power. The input-referred noise generators of basic transconductors have been derived using the approach for noise analysis of 2-port networks whereas those of active inductors have been obtained using the approach for noise analysis of 1-port networks. The linearity of active inductors has been investigated. Because active inductors are active networks that are sensitive to both supply voltage fluctuation and parameter spread. We have used supply voltage sensitivity and parameter sensitivity to quantify the effect of these unwanted variations. A distinct characteristic of active inductors is the dependence of their performance on the swing of their signals. When active inductors are used in applications such as LC oscillators where signal swing is large, the effect of this dependence must be accounted for.

The second part of the chapter has focused upon the CMOS implementation of gyrator-C active inductors. The schematics and characteristics of single-ended and floating (differential) class A active inductors have been investigated in detail. Class AB gyrator-C active inductors have also been studied. The basic gyrator-C active inductors suffer from a small parasitic parallel resistance and a large parasitic series resistance due to the small output / input impedance of the transconductors constituting the active inductors. This in turn lowers the quality factor of the active inductors. To increase the parallel parasitic resistance and to lower the parasitic series resistance, transconductors with a large input / output resistance are critical. This can be achieved by changing the configuration of transconductors, such as Karsilayan-Schaumann active inductors that have a large output impedance, employing cascodes, or adding parallel negative resistors. To increase the tunability of active inductors, additional voltage-controlled capacitors can be employed at critical nodes of active inductors. This approach is often preferable over those that vary the transconductances of the transconductors of active inductors because the latter also alters other parameters of the active inductors such as inductance with a downside that the tuning range is rather small. Feedback resistance active inductors, both single-ended and floating, exhibit improved performance by increasing the inductance and decreasing the series parasitic resistance simultaneously. Both improve the quality of the active inductors. To increase the voltage swing of the active inductors without sacrificing linearity, class AB active inductors constructed from a pair of nMOS/pMOS-configured class A active inductors have been presented. Two main drawbacks of class AB active inductors are the circuit complexity of these inductors and their need for a high supply voltage.