2

LOW POWER CMOS DESIGN FOR RADIO FREQUENCIES

In Chapter 1, an integration/power tradeoff was identified as one main obstacle to the implementation of small, cheap, low power transceivers for wireless sensor networks. This chapter describes the circuit design philosophies that have been developed to address these tradeoffs.

An important metric for RF blocks is the transconductance, which typically determines the total current consumption of the circuit. This chapter begins with a discussion of weak inversion circuit design, which is an increasingly relevant way of achieving efficient transconductance and is becoming more feasible with each technology node. Next, combining MEMS components with CMOS circuitry is shown to greatly reduce the reliance on external passive components. Three proof-of-concept chips are discussed to demonstrate the validity of these design strategies:

1. Circuit Proof-of-Concept I: 300μW Pierce BAW-Oscillator
2. Circuit Proof-of-Concept II: Differential 300μW BAW-Based Oscillator
3. System Proof-of-Concept: Energy Scavenging Transmit Beacon

We now turn to a discussion of weak inversion CMOS for Radio Frequencies.

2.1 Weak Inversion RF CMOS

As technology scaling relentlessly provides increasing digital clock frequencies, the effects on analog/RF circuit design continue to accumulate. Aggressive supply voltage scaling impedes the implementation of high dynamic range A/D converters and other precision analog circuitry. However, the increasing thickness and reduced resistivity of the copper metallization, coupled with the increased distance of these traces to the lossy substrate, allows the fabrication of high quality inductors and transmission lines. Subthreshold circuit design has been identified as a powerful tool in reducing the power consumption of

the transceiver. Weak inversion circuit biasing has been used for years in low frequency analog circuit design [10] to achieve increased transconductance efficiency. However, increasing transistor f_Ts allows weak-inversion operation in some RF circuit blocks. The inversion coefficient (IC) describes the relative level of channel inversion, which is most easily determined by the device current density. As the current density decreases, the transconductance efficiency increases. Equation 2.1 shows the inversion coefficient as a function of the transistor process parameters and operating point.

$$IC = \frac{I_d}{2nk'\frac{W}{L}V_t^2} = \frac{I_d}{I_o S} \tag{2.1}$$

Where n is the subthreshold slope factor, $k' = \mu C_{ox}$, $V_t = \frac{KT}{q}$, I_o is the specific device current, and S is the transistor aspect ratio. See Figure 2.1 for the transconductance efficiency vs. the inversion coefficient (IC) for a commonly used 0.13μm process [11].

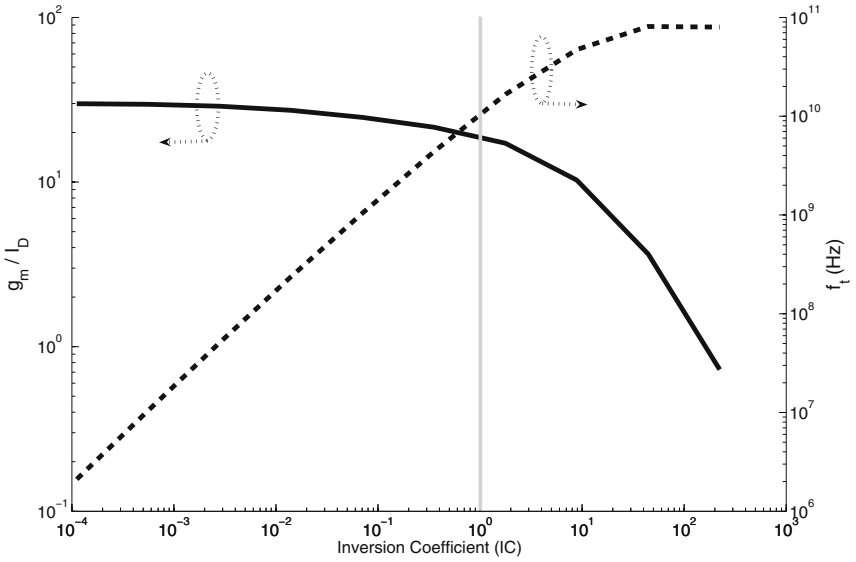

Fig. 2.1. The transconductance efficiency is plotted vs. the inversion coefficient (Courtesy of Nathan Pletcher)

The plot clearly shows the increase in transconductance efficiency as the inversion coefficient decreases. The line at IC = 1 is considered the middle of moderate inversion. Since the performance of many RF circuit blocks is directly related to device transconductance, it is advantageous to maximize the

transconductance efficiency of all critical devices in order to reduce the necessary bias current. However, reducing the current density also results in a severely decreased device f_T. An optimization of the current density is required to provide the correct balance between transconductance efficiency and bandwidth. Plots such as Figure 2.1 are useful tools for designers when choosing appropriate transistor bias points. Technology scaling allows greatly increased f_T realization for a given IC. Thus, weak inversion biasing for RF design will become increasingly useful in future technology nodes.

Throughout this work, the IC of critical transistors will be discussed. Most of the RF devices are biased in moderate to weak inversion to achieve enhanced transconductance efficiency and reduced bias current.

2.2 MEMS Background

The relatively new field of Radio Frequency Microelectro Mechanical Systems (RF MEMS) provides unique opportunities for RF transceiver designers. This section provides background on RF MEMS and provides insight into the opportunities presented by these new technologies. The field of RF MEMS includes the design and utilization of RF filters, resonators, switches, and other passive mechanical structures constructed using bulk processed integrated circuit fabrication techniques. To date, these devices have been commercially used as discrete board-mounted components, primarily used to enhance the miniaturization of mobile phones. However, RF MEMS components have the potential to be batch fabricated using existing integrated circuit fabrication techniques. Recent capacitively driven and sensed structures offer the potential of integration on the same substrate as the CMOS circuitry. In addition, because the resonant frequency of the structure is set lithographically, rather than by a deposition layer thickness, it is possible to fabricate devices with many unique resonant frequencies on the same die. A good example of this is presented by Bircumshaw in [12]. This resonator was constructed of micromachined polysilicon on a silicon wafer, providing good RF performance and the possibility of integration with active circuitry. The continued improvement in the performance, reliability, and manufacturability of these structures will greatly change the performance and form-factor of RF transceivers by allowing the reliable fabrication of advanced mechanical structures on the same substrate as the circuitry. However, as will be shown in this chapter, these devices hold the potential to enable new circuit blocks and architectures even in their present state as off-chip components.

At the onset of this project, RF MEMS was identified as an emerging technology with the potential to benefit low power RF transceivers. These devices provide three main benefits to circuit designers:

1. **High quality factor (Q) resonant structure.** BAW resonators can achieve quality factors greater than 1000, about 100X higher than on-chip

LC resonators. The resulting increased RF filtering ability both reduces oscillator phase noise and reduces frequency pulling/pushing of oscillators. When used in the design of bandpass filters and duplexers, high Q resonators help to realize the steep skirts necessary to meet cell phone specifications [13]. High Q resonators are further useful in a variety of other transceiver blocks. For example, high Q resonators provide the potential for radio frequency channel select filtering, as their bandwidth is much narrower than what can be obtained from integrated LC filters. This passive channel select filtering can be exploited to simplify the receiver architecture and to reduce the number of active components. In addition, when used in an RF oscillator, RF MEMS resonators provide a vastly improved phase noise compared to a standard, low Q LC resonator [14].

2. **Passive RF frequency reference.** For all narrowband communication systems, an RF carrier frequency generator is necessary. The absolute frequency reference used is typically a low frequency quartz crystal oscillator. The low frequency sinusoid is then multiplied up to radio frequencies by a frequency synthesizer. This technique has a few disadvantages for low power radio design. First, even for a fully integrated frequency synthesizer, an off-chip quartz crystal is always necessary, rendering true full integration impossible. In addition, frequency synthesizers are a large source of power dissipation in low power radios [7]. The VCO and frequency dividers tend to dominate the power consumption of frequency synthesizers. Radio frequency MEMS components provide an inherent high-frequency reference without the need for a power hungry frequency synthesizer.
3. **CMOS/MEMS co-design.** Since MEMS structures are fabricated using the same thin-film fabrication techniques as integrated circuits, each device may be custom-designed for its intended application. This provides additional degrees-of-freedom to the circuit designer. Unlike quartz crystals or discrete 50Ω filters, this flexibility allows the circuit designer to control impedance levels for minimal power consumption. One of the most exciting aspects of RF micromachined components is the potential for co-designing the MEMS devices with the CMOS circuitry. Until now, passive components are either low quality on-chip devices (inductors, capacitors) or high quality off-chip components (inductors, SAW filters, quartz crystals, duplexers). The on-chip components allow customization to meet the requirements of the circuitry, but their performance is usually poor. Meanwhile, high quality off-chip passives offer few designer degrees of freedom. For example, most filters and duplexers are designed for 50Ω input and output impedances. This rigid impedance level is very detrimental from a low power point of view, and has been extremely troublesome in past receiver implementations [15]. The potential of integrating RF MEMS components and circuitry on the same die or on the same substrate using, for instance, fluidic self assembly (FSA) could allow the circuit designer to size the MEMS components and the circuitry simultaneously [16].

> The ability to design these devices alongside the circuitry provides increased system performance and additional designer degrees of freedom.

Currently, many industrial and academic institutions have begun development of RF MEMS resonators. One promising technology is the Bulk Acoustic Wave (BAW, FBAR) piezoelectric resonator [17]. Recent work by Aissi has demonstrated the integration of an FBAR resonator on the same substrate as a BiCMOS oscillator [18], possibly foreshadowing the eventual practice of foundries offering MEMS process options. In this section we will provide a description of the structure and electrical model of a bulk acoustic wave resonator.

The FBAR employs a metal-piezo-metal sandwich to achieve a high frequency, tightly controlled second order resonance with an unloaded Q of approximately 1200. As shown in Figure 2.2, the resonator can be modeled as a series LCR circuit, with a series resonance occurring at $f_s = \frac{1}{2\pi\sqrt{L_x C_x}}$, with typically resonant frequencies ranging from 500MHz to 5GHz. Capacitor C_o

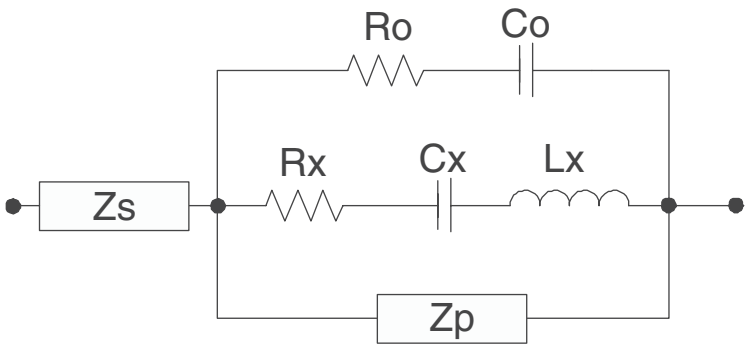

Fig. 2.2. Simplified circuit equivalent model of a BAW resonator

represents a parasitic feedthrough capacitance created by the parallel plates of the resonator. R_o models the finite quality factor of the feedthrough capacitance. Z_s and Z_p represent the loading effects of the CMOS circuitry on the resonator. These external impedances have a large effect on the resonator quality factor, resonant frequency, and frequency stability. In current applications, FBARs are combined into ladder structures and used as duplexers and bandpass filters for wireless applications [17]. Used in this manner, a much smaller form factor is achieved over traditional RF duplexers and filters. For low power transceivers, it is desirable to use single resonators to achieve a high quality factor and very narrow bandwidth. Referring to Figure 2.2, it is possible to distinguish two different resonant modes. The first, occurring at the *series resonance*, allows a low impedance path through the resonator at RF frequencies. At the series resonance, the effective series impedance is approximately

R_x. Above the series resonance, the structure looks inductive and will naturally tune out any parallel capacitive elements. This produces the *parallel resonance*, which occurs approximately 20MHz above the series resonance. At the parallel resonance, there is a circulation of RF current through the resonator and the feedthrough capacitor C_o. Due to this current circulation, at the parallel resonance the impedance of the structure increases dramatically to a value approximately 3 orders of magnitude higher than the *series resonance*. To avoid detuning the resonator in the series resonant mode, the impedance added to the resonator by the electronics (Z_s) must be small compared to R_x, or a few ohms. This is typically not possible using low power RF design techniques, where high impedances are necessary to reduce the current consumption. To avoid detuning the parallel resonant mode, the shunting impedance presented by the electronics (Z_p) must be much higher than the resonator impedance at parallel resonance (approximately 2kΩ). Thus, for low power RF transceiver design, it is desirable to operate on the parallel resonance of the resonator [19]. It should be noted, however, that the intrinsic quality factor of the series resonance will be higher than the parallel resonance due to the additional resistive losses of the circulating RF current.

The frequency stability of high Q resonators is a key feature that provides much more reliable operation that other LC-based frequency generators. Equation 2.2 shows the sensitivity of the parallel resonance[1] to capacitive variation.

$$\frac{\delta f_p}{\delta C_T} \simeq f_{series} \frac{-C_x}{2C_T^2} \tag{2.2}$$

C_T describes the total capacitive loading on the resonator This equation corresponds to a sensitivity of approximately -10kHz/fF of frequency variation due to process, temperature, or non-linear capacitor bias point shift. Equation 2.3 shows the frequency sensitivity of an LC tank to capacitive variation.

$$\frac{\delta f}{\delta C_T} = \frac{-C^{-3/2}}{4\pi\sqrt{L}} \tag{2.3}$$

For a tank defined by a 5nH inductance at 2GHz, a typical value for a fully-integrated oscillator, the frequency sensitivity is -856kHz/fF, nearly two orders of magnitude higher than the BAW resonator. Thus, an LC resonance would always need to be frequency locked to a reference even if perfect frequency accuracy were possible. In contrast, a BAW resonator, if sufficient accuracy were available, would not need to be frequency locked. This is a fundamental benefit of using high Q MEMS resonators in low power transceivers.

[1] And thus the subsequent oscillation frequency.

2.3 Circuit Proof-of-Concept I: 300μW Pierce Oscillator

To demonstrate the concepts presented in Sections 2.2 and 2.1, a proof-of-concept circuit was designed, implemented, and measured in a 0.18μm standard CMOS process [14] [19]. The goals of this project were threefold:

- A proof-of-concept circuit would verify the resonator/CMOS models and the co-design methodology. This verification is necessary as the accuracy of the models for MEMS components and weak inversion CMOS at RF frequencies are not as heavily developed as the traditional models for strong inversion CMOS circuitry, which designers have become accustomed to.
- A prototype would allow the refinement of the unresolved resonator/CMOS packaging and interconnect problem.
- This circuit, when used as a local oscillator, would also provide a stepping-stone to the implementation of an entire low power transceiver.

This section describes the state-of-the-art in transceiver local oscillator design. Used to generate the transmitted carrier frequency and the local oscillator (LO) signal, a stable, low-noise RF sinusoid generator is crucial for the performance of an RF link. Traditionally, this signal is obtained through frequency synthesis, which entails multiplying the frequency of a stable low frequency crystal oscillator via a phase- or delay- locked loop (PLL or DLL) [20]. There are, however, serious drawbacks with a frequency synthesizer. First, due to the low Q of the voltage controlled oscillator (VCO) tank and finite loop bandwidth of the PLL, the phase noise of the crystal oscillator is severely degraded by the frequency synthesizer. Secondly, the synthesizer consumes large amounts of power in the VCO and frequency dividers.

A few examples are useful for putting the problem in perspective. In a recent ultra low power frequency synthesizer design, approximately 400μW was consumed to provide a 434MHz carrier [7]. As the carrier frequency of these systems is increased into the GHz range, the power consumption of the frequency synthesizer increases dramatically. Outstanding phase noise performance can be achieved at the expense of high power dissipation. A recent high-performance 900MHz frequency synthesizer consumed 130mW with a phase noise of -127$\frac{dBc}{Hz}$ at a 330kHz offset [20]. The start-up time of a traditional frequency synthesizer is relatively long, and can be very inefficient if the transceiver requires agile duty-cycling and short packet transmission. Additionally, even with a "fully integrated" synthesizer, an off-chip quartz crystal is always required. Crystal oscillators typically exhibit very low phase noise due to the high quality factor of the crystal resonator. However, the resonant frequencies of quartz crystals are lower than most desired carrier frequencies, so frequency synthesis is usually required. A recent crystal oscillator implementation reports a phase noise of -113$\frac{dBc}{Hz}$ at 300Hz offset for a 78MHz oscillation frequency with a power dissipation of 340μW [21].

Another option is to use an integrated free-running LC-oscillator without a frequency reference. This could satisfy the need for a fast start-up time and

low power dissipation, but the frequency variation and phase noise of such a design would be prohibitively poor. In [14], we presented an alternate method of sinusoid generation. A frequency reference is generated directly at the RF frequency of interest, with no low frequency reference. This is accomplished by placing a BAW resonator in the feedback path of a CMOS oscillator, ultimately combining the frequency stability of a mechanical resonance with the low power capability of standard submicron CMOS. The technique of co-designing the resonator with the CMOS electronics provides an extremely low power solution.

In this design, a single resonator is used to maximize the loaded Q of the oscillator. The impedance of the resonator is less than 5Ω at series resonance and larger than 1500 ohms at parallel resonance. Thus, to avoid severely loading the natural Q of the resonator, operation at the parallel resonance of the FBAR was chosen. The resonator occupies an area of approximately 100μm x 100μm and is wire-bonded directly to the CMOS chip containing the circuitry. The Pierce oscillator topology was chosen for its low phase noise potential and because it operates on the parallel resonance of the FBAR, allowing a higher loaded Q. A circuit schematic of the oscillator is shown in Figure 2.3. The signal is DC coupled to the first stage of the output buffer (M_{buf1}). Capacitors C_1 and C_2 represent the device, interconnect, and pad

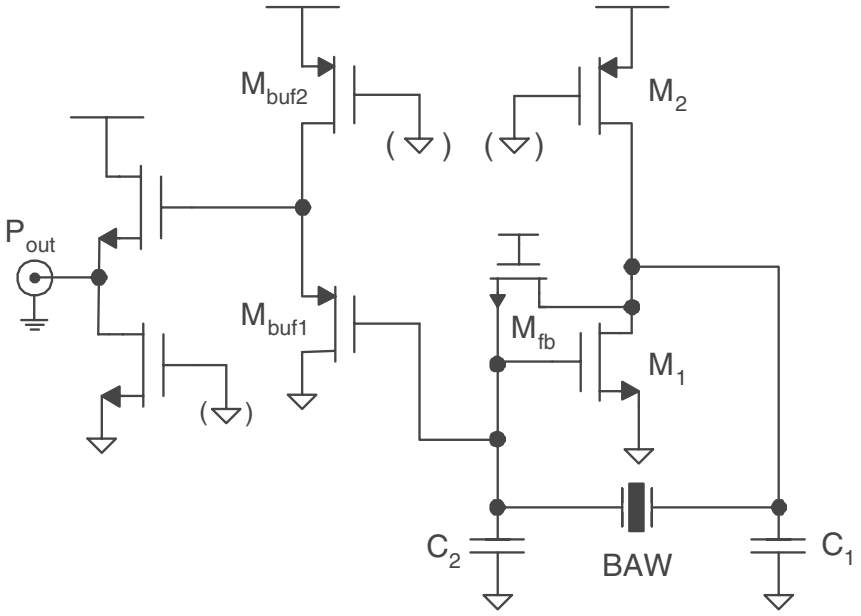

Fig. 2.3. Simplified oscillator schematic

capacitances. Accurate modeling and prediction of these values is crucial for the high frequency implementation of this topology. Transistor M_{fb} acts as a large resistor to provide bias to M_1. At the parallel resonance of the resonator, C_1, C_2, and C_o are tuned out. M_1 sees a high impedance at its drain node, allowing oscillation at this frequency. The sizing and layout of the circuit and resonator was optimized to minimize the power consumption of the oscillator.

At resonance, the initial loop gain is $A_L = g_{m1} R_L \frac{C_1}{C_2}$ where R_L is the real impedance seen at the drain of M_1 at the parallel resonance of the resonator. It can be shown that the optimal frequency stability and start-up factor are achieved with $C_1 = C_2$ [22]. Therefore, to minimize the transconductance necessary for oscillation and to maximize the output voltage swing for a given bias current, R_L was maximized. For a given frequency, BAW resonators may be designed with various membrane areas. As the area increases, the motional resistance (R_x) decreases. However, increasing the area also increases the feedthrough capacitance C_o. Increasing R_x degrades the loaded Q of the oscillator, thus decreasing R_L. Increasing C_o has a similarly detrimental effect. Thus, it is possible to calculate an optimal resonator area that minimizes the power dissipation and phase noise of the oscillator. Figure 2.4 plots R_L vs. the normalized resonator area for various values of $C_1 = C_2$. Using this technique, an optimal resonator area of approximately $(100 \text{ x } 100)\mu\text{m}^2$ was chosen for fabrication. The curve marker in Figure 2.4 indicates the design point. It is important to note that the finite Q of the CMOS device and pad capacitance must be taken into account, as they also reduce the loaded Q of the oscillator. This optimization led to a maximized value of R_L at parallel resonance. The desired voltage swing of the oscillator was 100mV zero-peak. The equation $V_0 = I_1 R_L$ relates the desired voltage swing to the first harmonic component of the drain current of M_1. Thus, since the oscillator is operated in the current-limited regime, the necessary oscillator core bias current is 300μA. As discussed in Section 2.1, weak inversion operation provides higher transconductance efficiency ($\frac{g_m}{I_d}$). The sizing of transistor M_1 (500/0.18)μm was chosen as to provide subthreshold operation, ensuring sufficient initial transconductance for reliable start-up. For transistor M_1, $IC = 0.2$, yielding $\frac{g_m}{I_d} = 23$.

A symmetric resonator layout allowed equal loading on the drive and sense electrode. The resonator was wirebonded directly to the CMOS chip to eliminate board parasitics, which would drastically degrade the resonator response. To accomplish this, the CMOS and BAW pad layouts were constructed with equal spacing so the chips could be mounted in close proximity to each other and directly wirebonded. See Figure 2.5 for a photograph of the completed prototype. The two chips were bonded with conductive epoxy to a grounded substrate, resulting in A 200μm spacing between the chips. A custom assembly with two bondwires per interconnect was used in the initial prototype to reduce the bondwire inductance, but subsequent experimentation showed that standard chip-on-board (COB) assembly using one bondwire per pad and a 500μm chip spacing was adequate. The oscillator core was biased at

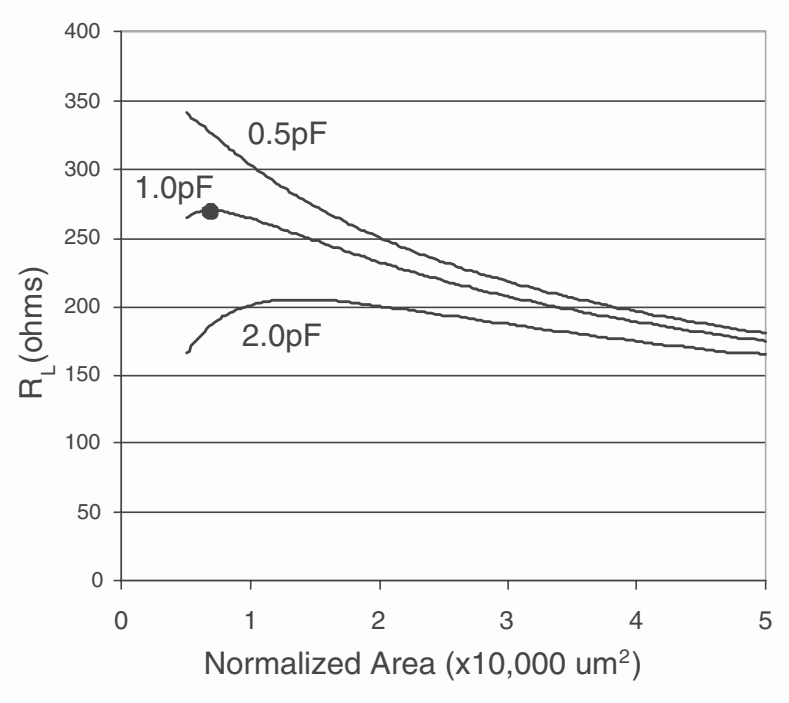

Fig. 2.4. Optimization of BAW resonator area. Three curves are shown with various values of $C_1 = C_2$

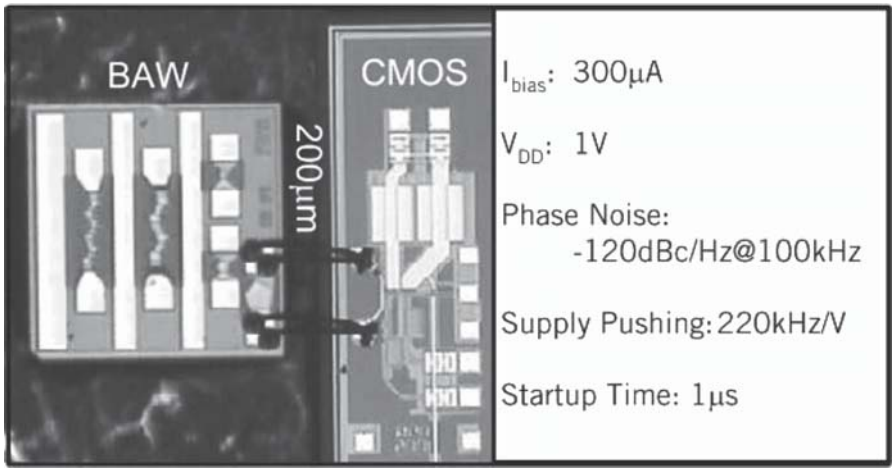

Fig. 2.5. Photograph of the CMOS/BAW prototype oscillator

300μA with a power supply voltage of 1V. The amplitudes of the 2^{nd}, 3^{rd}, 4^{th}, and 5^{th} harmonics were measured to be 30dB, 36dB, 45dB, and 49dB below the carrier, respectively. The measured phase noise performance is shown in Figure 2.6.

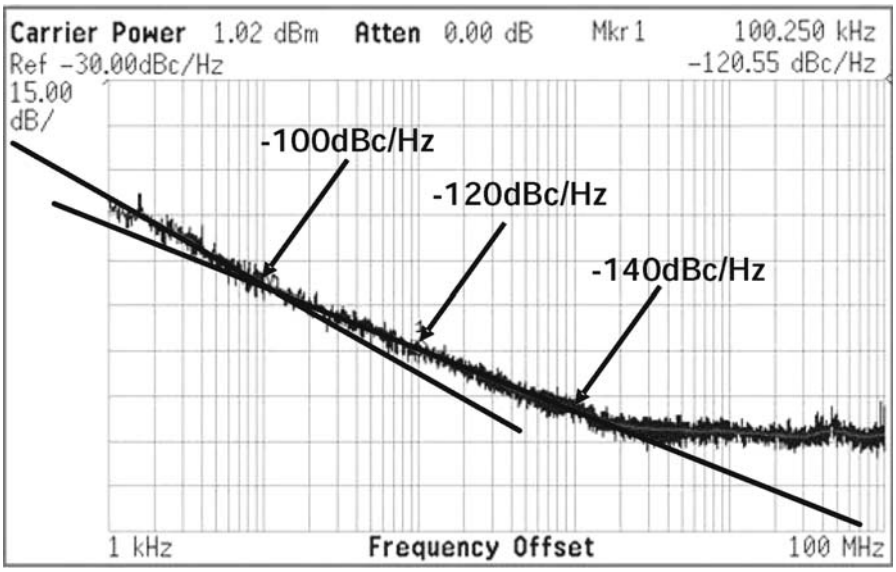

Fig. 2.6. Measured phase noise performance of the oscillator

Phase-noise was measured with an *Agilent E4445A PSA* and verified with an *HP 3048A* phase noise measurement system. The measured phase noise of the oscillator is -100 $\frac{dBc}{Hz}$ at 10kHz offset, -120 $\frac{dBc}{Hz}$ at 100kHz offset, and -140$\frac{dBc}{Hz}$at 1MHz offset. The start-up time of the oscillator was measured to be approximately 800ns, making it suitable as a frequency reference for receivers requiring agile duty-cycling. For example, it is possible to cycle the oscillator on/off between transmitted bits for low data rate OOK transceivers. Indeed, this property forms the basis for the transmitter that will be presented in Chapter 3. In addition, it was experimentally verified that analog pulse shaping of the OOK signal is possible by modulating the bias current of the oscillator as a function of time. Second, third, and fourth-generation oscillators have been fabricated and tested in a 0.13μm CMOS process, and similar performance results were observed. The supply pushing of the oscillator was measured to be 220$\frac{kHz}{V}$, yielding only a 26.4kHz frequency shift over a 10% supply voltage variation. The temperature coefficient of oscillation was also measured. A plot and detailed discussion of the effect of temperature on the oscillator is presented in Section 2.4, Figure 2.14. A useful figure-of-merit FOM for comparing the performance of RF oscillators is given by Equation 2.4 [23].

$$FOM = 10log\left[\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{L(\Delta\omega)\cdot V_{DD}\cdot I_{DD}}\right] \tag{2.4}$$

This FOM was used to compare some recently published low power RF oscillators. Table 2.1 shows a breakdown of oscillator performance and FOM for these oscillators. This table depicts low power oscillators using a variety

Table 2.1. Comparison of recently published RF oscillators

Parameter	This work [14]	[7]	[23]	[24]
Power Consumption (μW)	300	230	1460	100
V_{dd} (V)	1	1	0.35	0.5
Oscillation Frequency (GHz)	1.9	0.4	1.4	1.9
Phase Noise ($\frac{dBc}{Hz}$ @ 1MHz)	-140	-118	-129	-114
FOM (dB)	210	177	190	190
Comment	BAW	SMT L	Integ. L	Bondwire L

of tuning elements, including surface mount inductors, on-chip integrated inductors, and bondwire inductors. As shown in the table, the co-design of BAW resonators and subthreshold-biased CMOS circuitry provides FOM performance at least two orders of magnitude above the state-of-the-art in RF oscillators.

Co-design and optimization of CMOS circuitry and RF MEMS components will become an increasingly important tool with the proliferation of this technology. The imminent integration of RF MEMS on the same silicon substrate as the CMOS will enhance the performance of the system as well as the need for co-design.

2.4 Circuit Proof-of-Concept II: Differential 300μW BAW-Based Oscillator

In Section 2.3, the co-design of a single-ended CMOS oscillator and BAW was presented. However, to achieve better supply rejection and higher output swings, a differential topology is often used. The goal of the work presented in this chapter was to design a differential BAW-based oscillator for direct comparison with the single-ended oscillator presented in Section 2.3. This section presents the design, implementation, and testing of a 300μW differential BAW based oscillator.

2.4.1 Analysis/Design

The goal of the differential oscillator is to drive the BAW resonator symmetrically and excite its parallel resonance while maintaining symmetry throughout

the oscillator. In many traditional integrated differential oscillators, the negative resistance of the sustaining amplifier is achieved through a cross-coupled transistor pair. Looking into the cross-coupled pair, a wideband, DC-to-RF negative resistance is created. To achieve oscillation at a certain frequency, a parallel LC load is used to provide a high impedance at that frequency. At this frequency, the total tank impedance is negative and oscillation occurs. Bias current can conveniently be provided through the same inductors that tune out the tank capacitance.

A mechanical resonator-based differential oscillator, however, is somewhat more complicated. The following issues had to be overcome for successful implementation:

- **Low Frequency Stability:** The resonator can be shunted across the cross-coupled pair, providing a high Q response at the parallel resonance to set the oscillation frequency. However, at low frequencies, the resonator presents a high impedance. Thus, the circuit would be DC unstable and latch-up like a comparator.
- **Loaded Q:** Bias current must be supplied to the cross-coupled pair without de-tuning the BAW resonator at RF frequencies. Thus, a high impedance circuit environment at high frequencies is necessary.
- **Common-Mode Control:** A high-impedance bias circuit requires additional feedback circuitry to stabilize the common-mode of the oscillator. In traditional RF oscillator designs, the inductor tuning elements make common-mode feedback unnecessary.

Current sources could be used to supply bias current to the cross-coupled pair without de-tuning the resonator, but latch-up would occur. One way to circumvent this problem is to design a high-pass response into the cross-coupled pair negative resistance. This is realized by using separate current sources for the cross-coupled pair and coupling the sources through a capacitor [25]. At low frequencies, the cross-coupled pair experiences a large degeneration, reducing the negative resistance. At high frequencies, the sources interact, providing full transconductance from the cross-coupled pair. The simplified schematic of the oscillator is shown in Figure 2.7. It can be shown that the differential impedance looking down into the cross-coupled pair is given by Equation 2.5.

$$Z_{cc} = \frac{-1}{g_{m1}}[1 + \frac{g_{m1}}{s2C_s}] \tag{2.5}$$

Thus, at high frequencies, the structure provides $\frac{-1}{g_{m1}}\Omega$ of negative resistance. The effect of varying values of C_s is shown by the simulation results in Figures 2.8 and 2.9. Figure 2.8 shows the AC analysis of the oscillator loopgain for various values of C_s, swept logarithmically from 500fF to 5pF. The high Q BAW resonator series and parallel resonance is clearly visible. The desired oscillation mode is at the 1.9GHz parallel resonance peak. There is also a low Q low frequency resonance visible in the response due to the inductive nature of the capacitively degenerated cross-coupled pair interacting with the

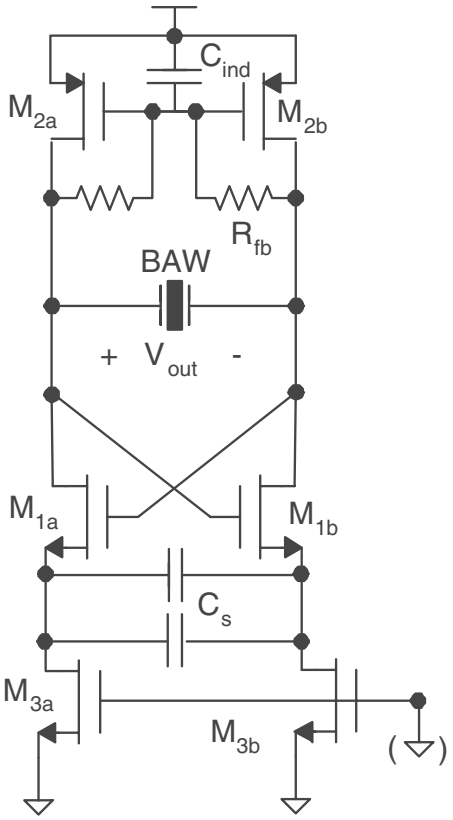

Fig. 2.7. Schematic of differential oscillator

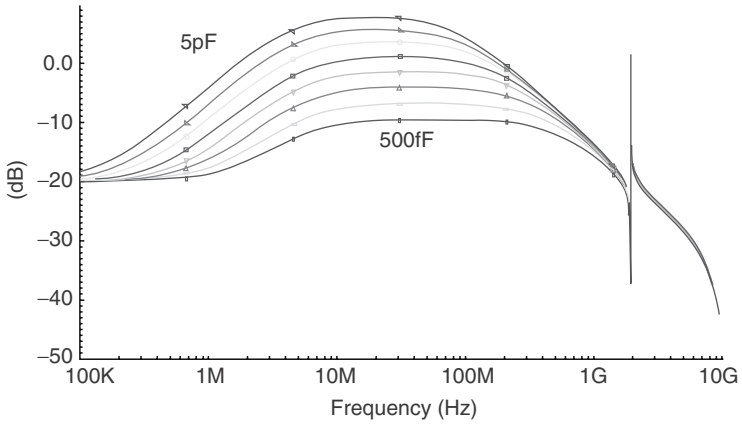

Fig. 2.8. Simulation results of oscillator loopgain for varying values of C_s

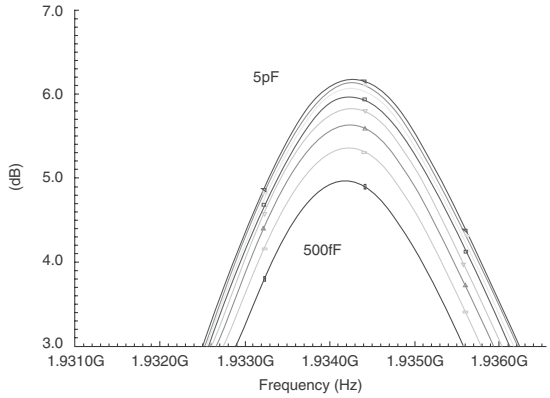

Fig. 2.9. Loopgain detail at oscillation frequency

BAW parallel plate capacitance. This resonance would cause a parasitic oscillation if the loopgain exceeded 0dB, and the stability would degrade as the parallel plate capacitance increased. To improve stability, C_s should be made small. However, reducing C_s increases the negative resistance pole frequency in Equation 2.5, thus reducing the oscillator loop gain at the desired resonance. Figure 2.9 shows a close-up of the oscillator loop gain at resonance for various values of C_s. The loop-gain degradation is clearly shown as C_s is decreased. Thus, proper choice of C_s is crucial for stable and efficient oscillation. For this oscillator, C_s=1pF was chosen to provide stable operation over a range of BAW resonators.

The next difficulty is achieving a stable common-mode voltage equilibrium. The common-mode feedback must not degrade the high frequency differential impedance of the current sources. To achieve a low LF common-mode impedance and a high HF differential-mode impedance, a self-biasing common mode feedback circuit was developed. This structure consists of M_{2a}, M_{2b}, R_{fb}, and C_{ind}. At low frequencies, the common-mode impedance looking into the inductor is $\frac{1}{g_{m2}}$. At RF, the differential impedance is $R_{fb}//R_{o2}$. Thus, the structure provides a stable DC common-mode operating point but does not de-tune the high Q BAW resonator. One drawback of the structure is that it consumes substantial supply headroom, limiting the low voltage operation potential of the oscillator. The common-mode voltage is easily adjustable by varying the aspect ratio of transistors M_{2a} and M_{2b}.

The sizing of the cross-coupled pair is an important consideration for achieving low power consumption. For oscillation, the transconductance of each device is dictated by the following: $g_m > \frac{2}{R_{p,res}}$. The sizing is a tradeoff between transconductance efficiency and f_T degradation in the weak inversion regime. The devices were sized at $\frac{100\mu m}{0.13\mu m}$, yielding an inversion coefficient of 0.33, providing a $\frac{g_m}{I_d}$ of approximately 21.

2.4.2 Experimental Results (1.9GHz)

To verify these concepts, the oscillator was implemented in a standard 0.13μm CMOS process. The layout detail is shown in Figure 2.10. The oscillator layout

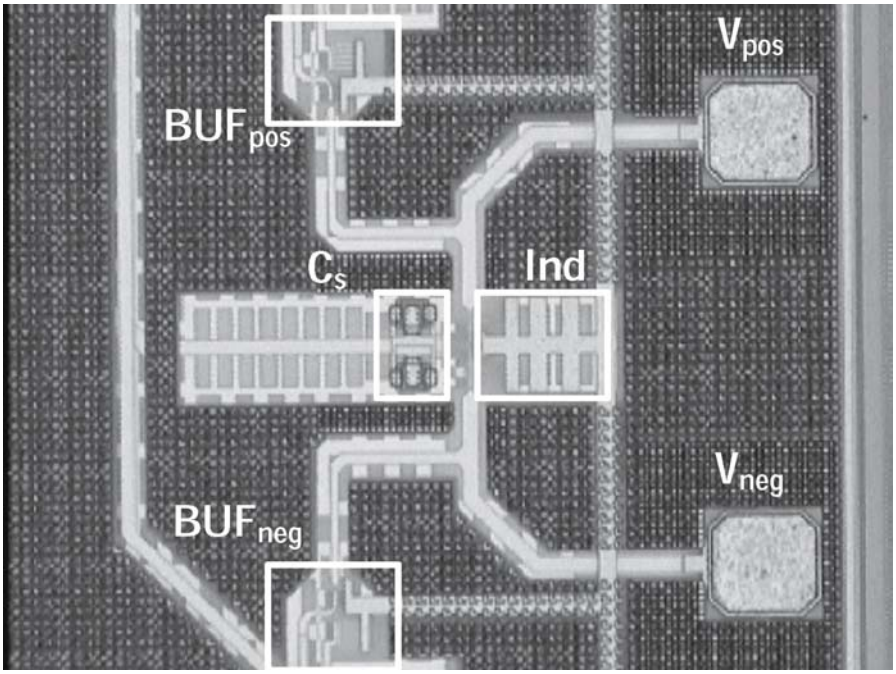

Fig. 2.10. Differential oscillator layout detail

was symmetric with a 290μm pad-to-pad spacing of the BAW interconnect pads. Both oscillator outputs are buffered with self-biased 50Ω output drivers that present a 100fF capacitance to the oscillator core. The active inductor structure and output buffers are visible in the photo. Capacitor C_s, also visible, was split into two cross-coupled capacitors to eliminate the asymmetry of the back plate connection. The oscillator layout is symmetric up to the buffer outputs, where an asymmetric pad structure was used for die area efficiency. A photograph of the oscillator COB assembly is shown in Figure 2.11. The board was assembled using standard COB techniques with no special processes required. The oscillator was then tested over various bias current levels. Oscillation was sustained at a bias current as low as 155μA total, corresponding to a g_m of approximately 1.6mS for each cross-coupled device. Thus, back-calculating the resonator parallel resonant impedance reveals $R_{p,resonator} = \frac{2}{g_m} = 1.2k\Omega$, agreeing well with calculations. The differential zero-peak swing for a 155μA bias current was 50mV. The output swing

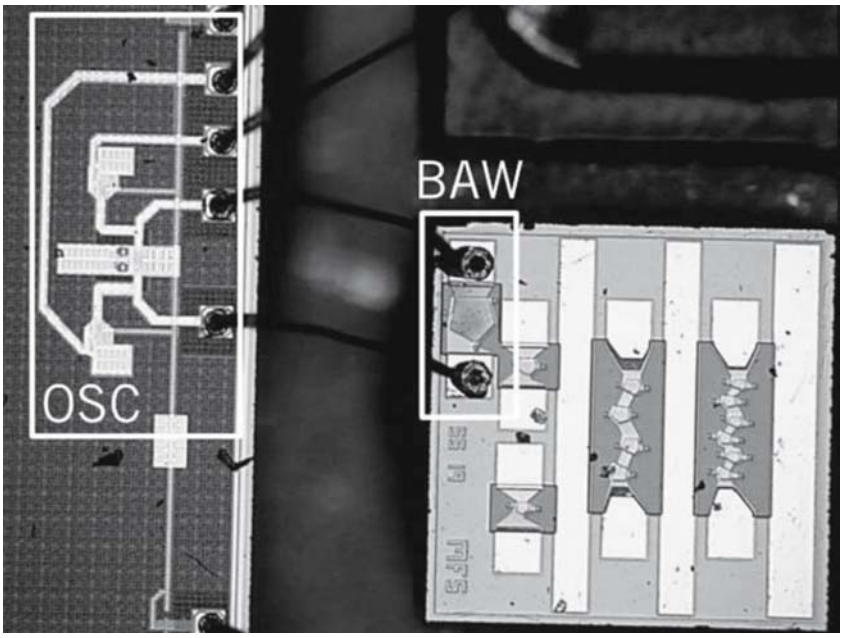

Fig. 2.11. Differential oscillator COB assembly

increased linearly with bias current up to a total bias of 600μA, where the differential voltage swing was 318mV zero-peak. As the current was further increased, the oscillator entered the voltage-limited regime and subsequent increases in bias currents resulted in diminishing increases in voltage swing.

Next, the oscillator was biased to the design value of 300μA (150μA through each leg) for the remainder of the testing, yielding a differential output power of -13.2dBm (corresponding to an oscillator core differential swing of approximately 200mV zero-peak). The phase noise was measured with an *Agilent E4445A PSA*. The data is plotted in Figure 2.12. A comparison of this phase noise measurement to that from the Pierce oscillator presented in Section 2.3 reveals interesting results. Since both oscillators operate with nearly equal differential voltage swings across the resonator (200mV zero-peak) and nearly equal resonator impedances, it follows that the power in the resonant tank is nearly identical. In addition, because the resonator quality factors are nearly equal, the phase noise of the both oscillators yield similar results when calculated with Leeson's formula.

Table 2.2 shows the phase noise comparison of the differential oscillator to the Pierce oscillator presented in Section 2.3.

Notice that the phase noise performances of the two oscillators are very similar. An oscillator supply-pushing performance of $500\frac{kHz}{V}$ was measured over a V_{dd} range of 0.7V to 1.4V. The low supply-pushing figure is due to the

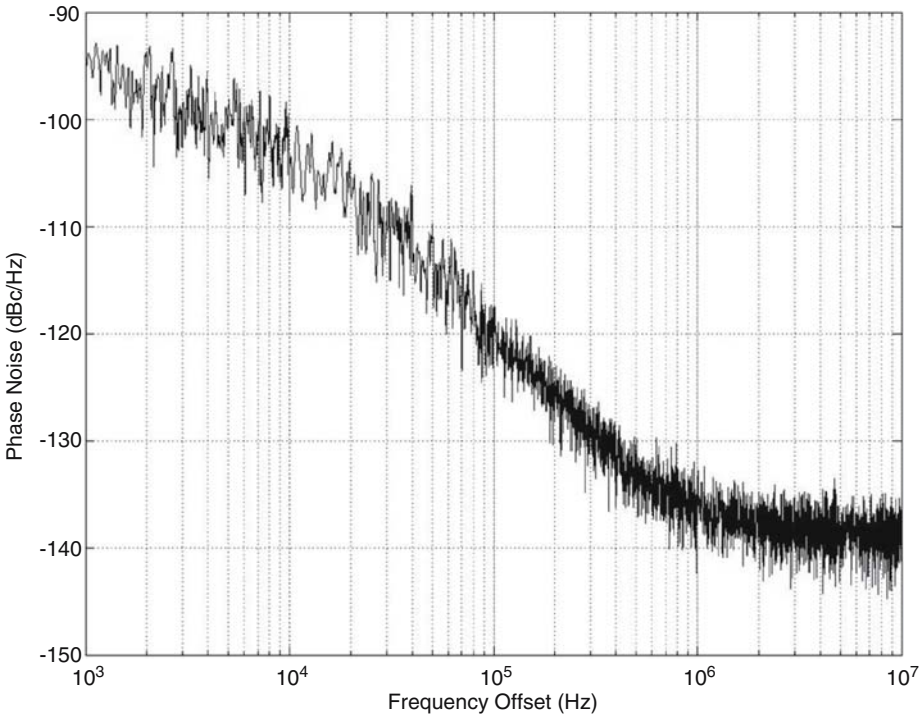

Fig. 2.12. Measured differential oscillator phase noise

Table 2.2. Measured oscillator phase noise ($\frac{dBc}{Hz}$)

f_{offset}(Hz)	Differential	Pierce
10k	-103.3	-100
100k	-120.3	-120
1M	-136.4	-140

low resonator frequency dependence to non-linear capacitor bias point shifts, as explained in Section 2.2. A 10% variation in the nominal 1.2V supply would result in only a 60kHz frequency shift.

The measured harmonic components of the differential and Pierce oscillators are compared in Table 2.3. As expected, the even order harmonics of the differential oscillator are suppressed by the differential architecture. The fourth harmonic was below the noise floor of the spectrum analyzer.

The start-up time of the oscillator was measured with an *Agilent 54855A* 8bit, 6GHz oscilloscope. Figure 2.13 shows the measured oscillator start-up transient. The positive and negative output voltages of the differential oscillator are shown. The start-up time, measured from the onset of bias current

Table 2.3. Measured oscillator harmonic distortion (dBc)

Harmonic	Differential	Pierce
Second	-55	-30
Third	-58	-36
Fourth	–	-45
Fifth	-65	-49

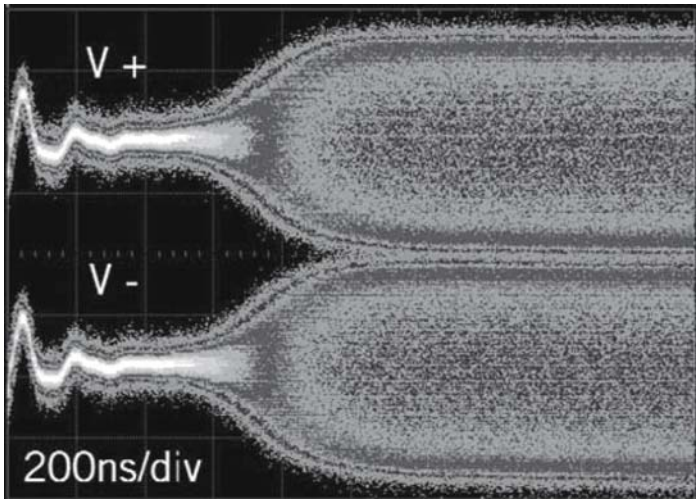

Fig. 2.13. Measured differential oscillator start-up transient

to oscillator saturation, is approximately 1μs. This matches, both theoretically and experimentally, the start-up time of the Pierce oscillator presented in Section 2.3. This result is expected because both oscillators have similar tank quality factors and initial loop gains.

The temperature dependence of a BAW-tuned reference oscillator is important because it is not locked to a stable temperature compensated crystal reference. As described in [26], the temperature coefficient of the parallel resonance of a Molybdenum/Aluminum Nitride/Molybdenum (Mo/AlN/Mo) BAW resonator is approximately -25$\frac{ppm}{^\circ C}$. For a high Q resonant structure, the resonator temperature coefficient should determine the temperature coefficient of oscillation frequency (TCF). To verify this relationship, the differential oscillator frequency was measured over a temperature range of -20°C to 100°C. This measurement was performed with a *Thermonics T-2420* temperature forcing system. In addition, the Pierce oscillator that will be used in Chapter 3 was measured over the same range for comparison. See Figure 2.14 for the measured results. The differential oscillator uses a custom-designed 70Ω resonator while the Pierce uses a 50Ω resonator test structure. The theoretical

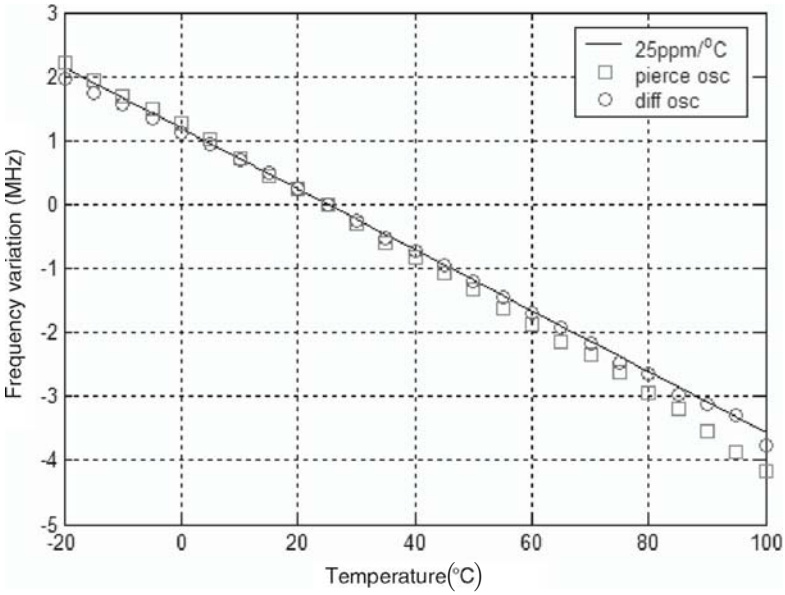

Fig. 2.14. Measured temperature coefficient of oscillation for two CMOS oscillators

-25$\frac{ppm}{^{\circ}C}$ curve was plotted for reference. As expected, the measured TCF of both oscillators closely match the theoretical resonator coefficient. The Pierce oscillator shows a slightly higher TCF that increases with temperature. This increase is due to the temperature dependence of the CMOS power amplifier that loads the oscillator. The addition of temperature-independent bias stabilization circuitry would return the curve to its theoretical TCF value. The linear, known TCF response may be easily compensated to provide a stable frequency reference. A compensation circuit providing approximately -5$\frac{fF}{^{\circ}C}$ to the resonator would provide temperature stability. In completely uncompensated form, both oscillators exhibit a +/- 1MHz tolerance from 5°C to 45°C.

The motional resistance of the BAW resonator also exhibits a temperature dependence [26]. Important to low power CMOS oscillators is the temperature coefficient of the parallel resistance, which affects the oscillator loop-gain, output swing, and phase noise performance. This temperature coefficient is approximately -1500$\frac{ppm}{^{\circ}C}$. Over a range of -20°C to 100°C, R_p decreases by approximately 18%. This relatively small variation is easily compensated by oscillator amplitude control circuitry.

2.4.3 Experimental Results (2.4GHz)

As designed, the differential oscillator can operate successfully over a wide frequency range with no modifications. One particularly interesting frequency band is the 2.4GHz ISM[2] band. This band is sufficiently high to allow completely integrated inductors, but low enough to allow subthreshold RF transistor biasing and low power consumption.

It should be noted that there is an optimal C_s for each oscillation frequency. As the frequency increases, the allowable cross-coupled pair pole frequency (given by Equation 2.5) can be increased, allowing a smaller C_s and thus higher stability against low frequency parasitic oscillations. A custom 2.4GHz resonator was designed and fabricated to demonstrate oscillator operation in this frequency band. Figure 2.15 shows a photograph of the completed ISM band oscillator implementation.

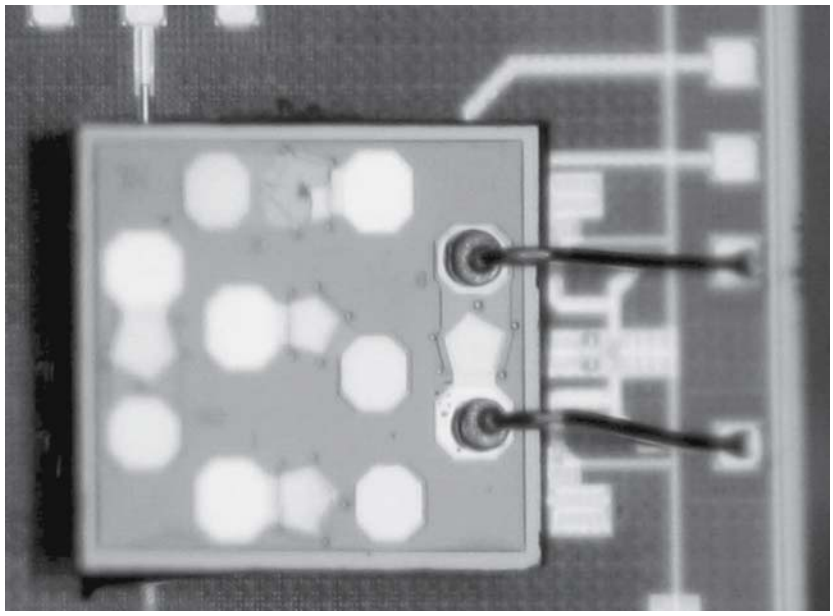

Fig. 2.15. ISM implementation of differential oscillator

The CMOS chip is shown below the BAW chip. The resonator chip was designed with five resonators. The four perimeter resonators are spaced in frequency across the ISM band. The resonator die (1mm x 1mm) was assembled on top of the CMOS die with non-conductive epoxy. Wirebonding provided

[2] Industrial, Scientific, and Medical

the electrical connectivity between the two chips. This experimental assembly methodology worked well and successfully de-coupled the CMOS/FBAR assembly and the CMOS/board assembly.

The oscillator was biased to 200μW per leg for stable startup (400μW total). This relatively high bias current is due to the quadratic relationship of bias current to the operation frequency, which predicts a 1.6x increase in startup transconductance. In addition, due to the experimental nature of the ISM-band resonators, high variation in resonator motional resistances were expected. Figure 2.16 shows the steady-state transient oscillator output. Oscillation occurred at 2.43GHz as expected. The oscillator exhibited a clean

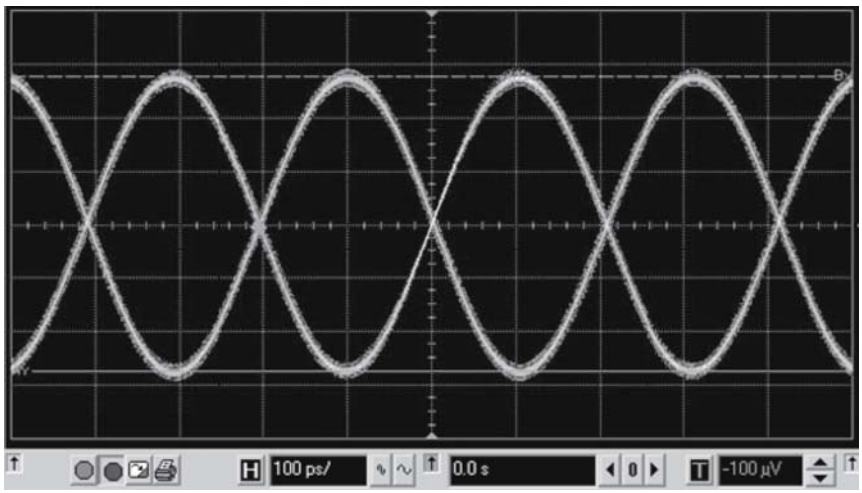

Fig. 2.16. ISM differential oscillator transient output

spectrum and good amplitude matching. The phase-noise of the oscillator was measured with an *Agilent E5052A* Signal Source Analyzer over four bias point settings (400μA, 500μA, 600μA, 700μA). See Figure 2.17. As expected, the close-in phase noise and noise floor decrease as the oscillator loop power increases. At a bias current of 400μA, the oscillator exhibits a phase noise of approximately $-113\frac{dBc}{Hz}$ at 100kHz offset. This is approximately 7dB higher than the previous 1.9GHz version of the oscillator, indicating a reduced resonator quality factor. The inferred quality factor of the resonator from these phase noise measurements is approximately 200.

This proof-of-concept demonstrates the practical application of MEMS and integrated circuit co-design techniques at higher frequency bands. Our current work in this area involves the design of a quadrature voltage controlled oscillator (QVCO) tuned by BAW resonators. This work will involve coupled RF oscillators to generate accurate quadrature sinusoids. Although the phase

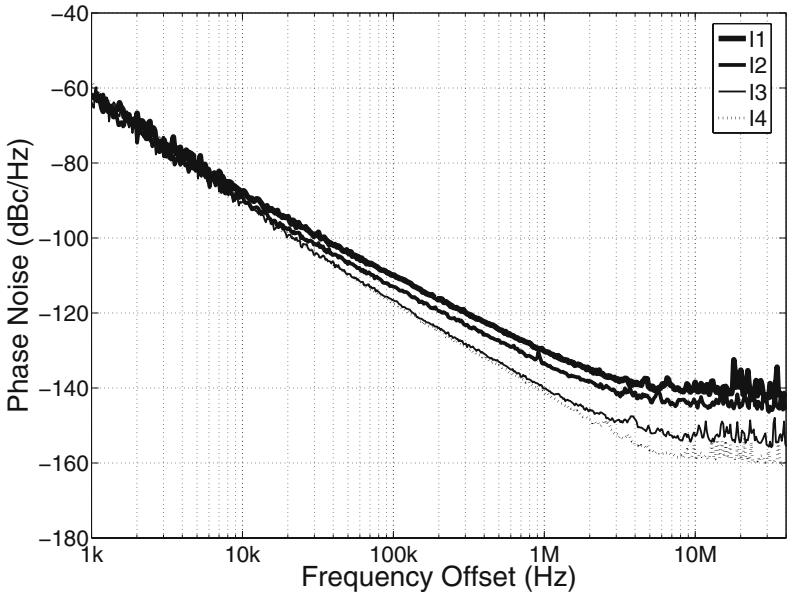

Fig. 2.17. ISM differential oscillator phase noise

noise performance will be significantly better than a traditional LC-tuned oscillator, a number of difficulties remain. First, the tuning range of high Q structures is fundamentally very low. To allow a reasonable tuning range, it is anticipated that a switched resonator array will be necessary in addition to capacitive tuning. Secondly, maintaining low phase error between the two oscillator cores is crucial. This phase error is determined (in part) by the center frequency offset the two resonators. When a high-Q resonant structure is used, the frequency alignment specifications become stringent, so adaptive calibration techniques are currently being explored to maintain high phase accuracy.

2.5 System Proof-of-Concept: Energy Scavenging Transmit Beacon

The previous section confirmed the design philosophies involved in co-designing BAW resonators and CMOS circuitry at RF frequencies. This section seeks similar confirmation of the system-level philosophies: *Can 1cm^3 energy scavengers realistically and robustly power GHz-range RF circuitry?* The ultimate goal of this work, as reported in [27] was to develop a completely self-powered

wireless node.[3] The two most applicable energy scavenging technologies are solar power and vibration-based power, due to the large potential application space of these technologies. Photovoltaic solar cells are a mature technology, and a solar cell based power source may be implemented using commercial off-the-shelf technology. In addition, the technique of utilizing low-level vibrations as a power source was also investigated.

This section reports a 1.9GHz transmit beacon that is successfully operational using solar and vibrational power sources. The main components of the design are the energy scavenging devices, the powertrain, the local oscillator, the power amplifier, and the antenna. One main goal was to maximize the efficiency of the conversion from solar and vibrational power to transmitted RF power. The power circuitry converts the scavenged energy into a stable supply voltage for the RF circuitry. This process entails converting a high impedance, unstable supply into a stable, low impedance 1.2V supply. A 10μF storage capacitor functions as an energy reservoir. When the capacitor charges to a pre-specified energy level, the supply rails to the RF circuitry are activated and energy is consumed. Because the transmitter dissipates power faster than the rate at which the piezoelectric generator or solar cell can produce it[4], the voltage across the storage capacitor falls when the radio is on. Once the energy has been depleted to a level specified by a "Shutdown control" block, the supply rails are disabled and the capacitor is recharged.

The choice of energy storage mechanism involves a tradeoff between energy density and reliability. Batteries have far higher energy density than do capacitors. For example, rechargeable lithium ion batteries have an energy density of roughly 1000 J/cm^3. Ceramic capacitors have an energy density on the order of 1 to 10 J/cm^3. However, most lithium ion batteries are limited to 500 to 1000 recharge cycles and have a finite shelf life. Furthermore, the life of the battery would suffer in the proposed application because the batteries are kept charged with a trickle of current rather than undergoing deep discharge. Capacitors, on the other hand, have an almost infinite lifetime and are simpler to charge. Because wireless sensor nodes do not require substantial energy storage, and because lifetime of the node is a primary concern, a capacitor was used.

Although a linear regulator would result in a lower total efficiency in the current design scenario, a linear regulator was chosen because of its ability for a higher level of integration and increased simplicity[5]. The transmitter was designed using the same CMOS/MEMS co-design philosophies described earlier in this chapter. A photo of the transmitter is shown in Figure 2.18. The entire transmit area consumes less than 20mm^2 of board space. The oscillator

[3] The work in this section was in collaboration with S. Roundy, Y.H. Chee, and P. Wright

[4] Except in direct sunlight

[5] No external filtering inductors or capacitors is needed, in contrast to switching regulators

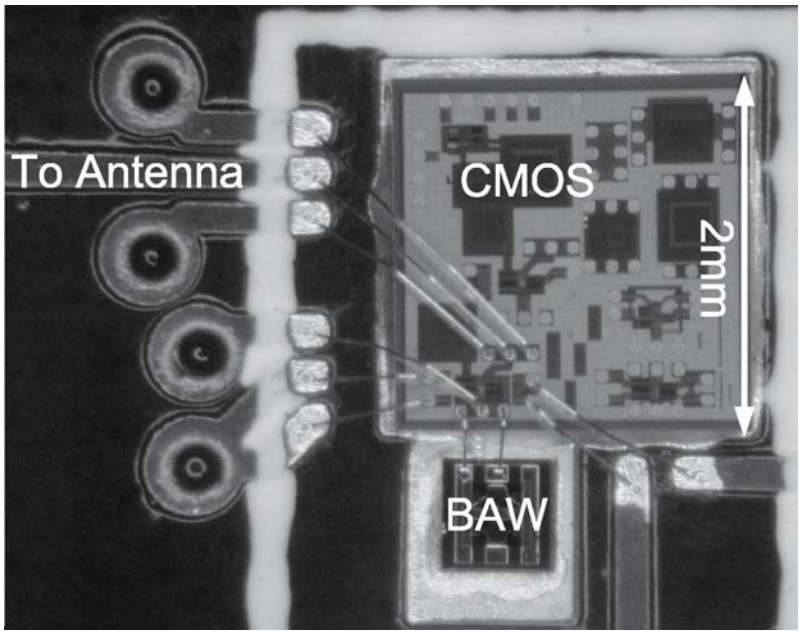

Fig. 2.18. RF Transmitter COB implementation

provides a 100mV signal to the integrated power amplifier, which provides a 0dBm signal to the chip antenna. An output power of -1.5dBm was measured in close proximity to the chip antenna. The completed $(2.4\,\mathrm{x}\,3.9)\mathrm{cm}^2$ transmit beacon implementation is shown in Figure 2.19. The powertrain, photovoltaic solar cell, transmitter, and 1.9GHz chip antenna are clearly visible. All circuitry is placed on the back of the board, allowing the front to be utilized for solar collection and RF emission. Although a commercial, off-the-shelf voltage regulator was used, a custom integrated circuit could provide higher efficiency and a much smaller board footprint[6]. A custom piezoelectric bender was also designed[7] to power the beacon. The bender exhibits a resonant frequency of approximately 200Hz and a quality factor of about 20. Thus, the output power drops off rapidly as the stimulus frequency drifts from the bender resonant frequency. Although not shown, the transmit beacon was successfully powered by this bender, demonstrating that hybrid energy scavenging is a viable option for wireless sensor networks.

See Figure 2.20 for the measured beacon voltage levels under low lighting conditions. V_{supply} is the voltage on the storage capacitor. Under low solar input conditions, this voltage slowly charges to a pre-defined level. At that voltage, the voltage regulator is enabled and V_{reg} rises to a stable 1.2V,

[6] This is a subject of current research
[7] Designed by Shad Roundy, U.C. Berkeley [3]

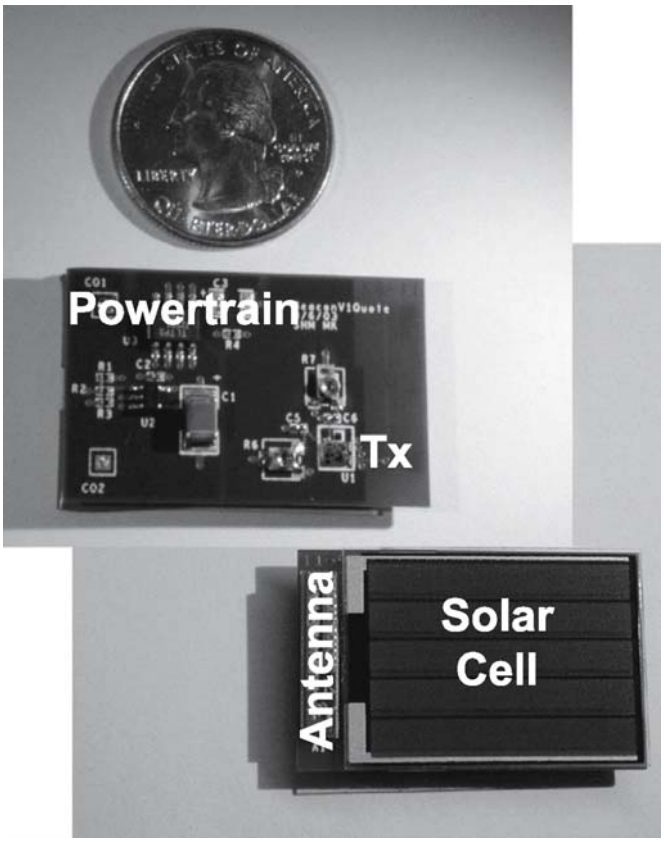

Fig. 2.19. Transmit beacon implementation

powering the RF transmitter. The RF blocks are then enabled, beginning transmission. During this stage, V_{supply} decreases as energy is drawn from the storage capacitor. When a sufficiently low level of capacitor energy is sensed, the voltage regulator is disabled and the RF transmission stops. The main figure of merit of this system is the transmit duty cycle under various environmental conditions.

The achievable transmit duty cycle varies dramatically over various lighting conditions. In the presence of low indoor light, the duty cycle is approximately 0.4% (400bps throughput assuming a 100kbps transmitter datarate). In direct sunlight, the duty cycle is 100% (in that condition, the solar cell is supplying more power than necessary for constant transmitter operation). For a $5.7m/s^2$ vibration level (about $0.58G$), the transmitter duty cycle is about 2.6%, corresponding to a throughput of 2.6kbps. The transmit beacon operates indefinitely from ambient energy and has been in continuous service for approximately 3 years.

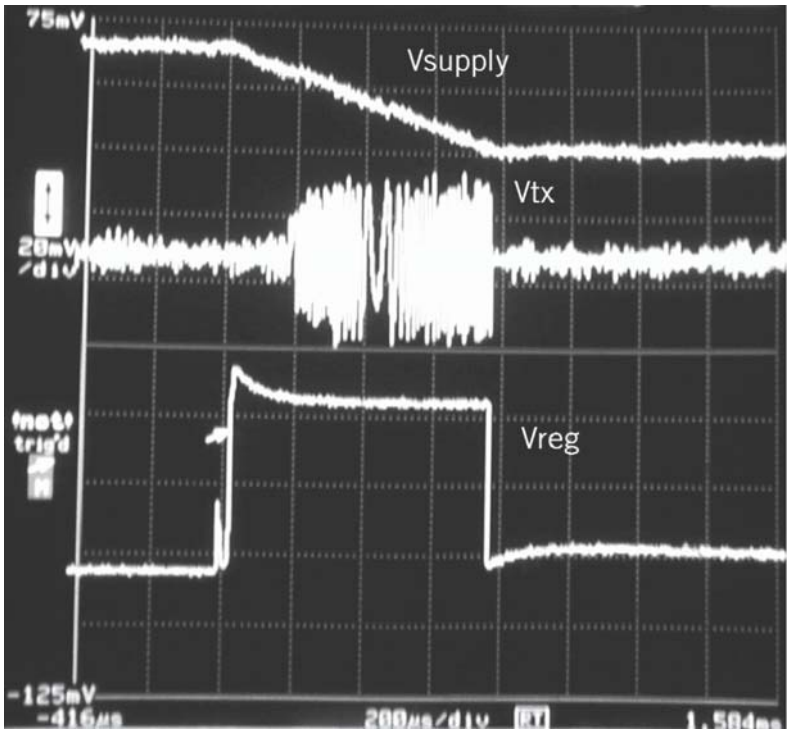

Fig. 2.20. RF transmit beacon under low light conditions