Chapter 2

DESIGN TECHNIQUES FOR CURRENT-MODE CIRCUITS

The rapid down-scale of the feature size of MOS devices, the aggressive reduction in the supply voltage, and the moderate reduction in the threshold voltage of modern CMOS technologies have greatly affected the performance of CMOS current-mode circuits, reflected by a small dynamic range, a reduced effective gate-source voltage, a low device output impedance, and an increased level of device mismatches. This chapter examines the design techniques that improve the performance of low-voltage CMOS current-mode circuits. The chapter is organized as follows : Section 2.1 examines the characteristics of basic current amplifiers. Section 2.2 investigates the techniques that boost the output impedance of current-mode circuits. Section 2.3 examines the techniques that lower the input impedance of current-mode circuits. Section 2.4 presents a balancing network approach for eliminating the mismatch-induced output offset current of current-mode circuits. In Section 2.5, an effective power reduction technique called current-branching is investigated. Section 2.6 introduces resistor series peaking, inductor series peaking, and current feedback for bandwidth improvement of current-mode circuits. Section 2.7 looks into circuit techniques for dynamic range improvement, specifically the characteristics of class AB current amplifiers. In Section 2.8, our focus is on the topologies and characteristics of CMOS active inductors. The applications of active inductors will be given in later chapters of the book. The chapter is summarized in Section 2.9.

2.1 Basic Current Amplifiers

The schematic of basic CMOS current amplifiers is shown in Fig.2.1(a). Because a well-designed current-mode circuit possesses a small input

impedance and a large output impedance, it is reasonable to assume that the load impedance is sufficiently small. As a result, M_2 is not subject to Miller effect. Under a perfect matching condition and neglect the channel length modulation, the current transfer function is given by

$$\frac{I_o(s)}{I_{in}(s)} = \frac{A}{\frac{s}{\omega_b} + 1}, \tag{2.1}$$

where $A = \frac{g_{m2}}{g_{m1}}$ and

$$\omega_b \approx \frac{g_{m1}}{C_{gs1} + C_{gs2} + C_{gd2}}. \tag{2.2}$$

The input impedance of the basic current amplifier is given by

$$z_{in}(s) = \frac{1}{g_{m1}} \left(\frac{1}{\frac{s}{\omega_b} + 1} \right). \tag{2.3}$$

The input impedance can be lowered by either increasing the width of M_1 or increasing the biasing current. The former lowers the bandwidth whereas the latter increases the static power consumption.

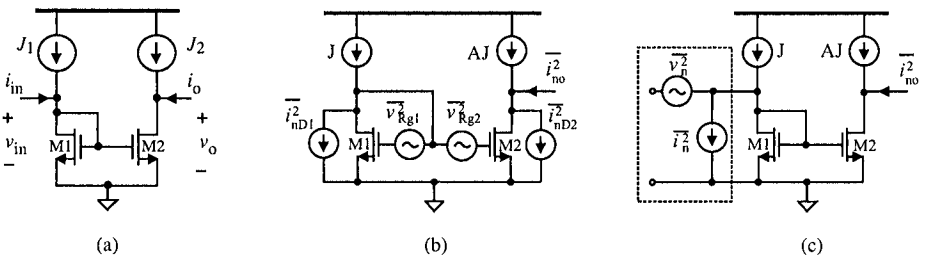

Figure 2.1. (a) Basic current amplifier; (b) Noise sources in basic current amplifier; (c) Input-referred noise-voltage and noise-current generators of basic current amplifier.

The output impedance is given by $z_o \approx r_{o2}$ approximately. It was shown in [27] that the output impedance of MOSFETs in deep sub-micron CMOS technologies is small. The finite output impedance of MOSFETs gives rise to a change of the output current i_o when the output voltage v_o varies. Because $i_o = g_{m2}v_{gs} + g_{o2}v_o$ and $i_{in} = (g_{m1} + g_{o1})v_{gs}$, we have

$$i_o = \frac{A}{1 + \frac{g_{o1}}{g_{m1}}} i_{in} + g_{o2}v_o$$

$$\begin{aligned} &\approx A(1-\frac{g_{o1}}{g_{m1}})i_{in}+g_{o2}v_o \\ &\approx Ai_{in}+g_{o2}v_o. \end{aligned} \tag{2.4}$$

The second term on the right hand side of (2.4) is the output error current.

The noise equivalent circuit of the basic current amplifier is shown in Fig.2.1(b,c). The equivalent channel noise of M_1 and M_2, denoted by $\overline{i_{n1}^2}$ and $\overline{i_{n2}^2}$ respectively, consists of (i) the thermal noise of the channel and (ii) the thermal noise of the gate resistance that is referred to the channel. Because circuits of our interests operate at high frequencies, the flicker noise of MOS transistors, which has a typical corner frequency of a few MHz, is neglected. As a result,

$$\overline{i_{n1,2}^2}=4kT(\gamma+R_{g1,2}g_{m1,2})g_{m1,2}\Delta f, \tag{2.5}$$

where R_g is the gate series resistance, $\gamma\approx 2.5$ for deep sub-micron devices, T is the temperature in degrees Kelvin, and k is Boltzmann constant. For a typical 0.18μm CMOS technology, the sheet resistance of silicided polysilicon (gate) is approximately 8Ω. If the dimension of the gate of a nMOS transistor is $L=100\mu$m and $W=0.18\mu$m with one-finger layout, then $R_g\approx 4.44k\Omega$. Assume $g_m=5$mA/V, we have $R_g g_m=22.2$. Clearly in this case the noise of the nMOS transistor is dominated by the thermal noise of the gate series resistance. To reduce the thermal noise of the gate series resistance, the multi-finger layout approach becomes mandatory. Consider that 4 fingers are used for the transistor, we have $L=25\mu m$ for each finger. Because these fingers are connected in parallel, $R_g\approx 1.11k\Omega$ and $R_g g_m\approx 5.5$, which is comparable to the value of γ.

Using conventional approaches for noise analysis, one can show that the power of the input-referred noise voltage and current generators, denoted by $\overline{v_n^2}$ and $\overline{i_n^2}$ respectively, are given by [28]

$$\begin{aligned} \overline{v_n^2}&=\frac{1}{g_{m1}^2}\left(\frac{\overline{i_{n2}^2}}{A^2}\right), \\ \overline{i_n^2}&=\overline{i_{n1}^2}+\frac{\overline{i_{n2}^2}}{A^2}, \end{aligned} \tag{2.6}$$

2.2 Output Impedance Boosting Techniques

2.2.1 Basic Cascodes

It was pointed out in the preceding section that the output error current of the basic current amplifiers can be minimized by maximizing the output impedance. Cascode configuration shown in Fig.2.2(a) employs

a negative voltage-current feedback to sustain the output current in the presence of a varying output voltage. The output impedance of the cascode current amplifier can be obtained from its small-signal equivalent circuit $z_o \approx (g_{m3}r_{o3})r_{o2}$.

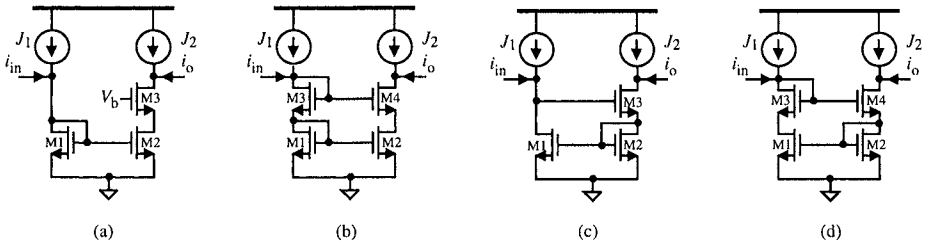

Figure 2.2. (a) Cascode current amplifier with an external biasing voltage V_b; (b) Self-biased cascode current amplifier; (c) Wilson current amplifier; (d) Improved Wilson current amplifier.

Let us examine the reduction in the output error current from the cascode. Writing KCL at the drain of M_2 yields

$$v_2 = \frac{g_{o3}v_o - g_{m2}v_{in}}{g_{o2} + g_{o3} + g_{m3}}. \tag{2.7}$$

Further $i_{in} = (g_{m1} + g_{o1})v_{in}$, $i_o = -g_{m3}v_2 + g_{o3}(v_o - v_2)$, and assume $g_m \gg g_o$, we have

$$i_o \approx A i_{in} + \left(\frac{g_{o2}}{g_{m3}r_{o3}}\right)v_o. \tag{2.8}$$

A comparison of (2.4) and (2.8) reveals that the output current error of the cascode current amplifier is $g_{m3}r_{o3}$ times lower than that of the basic current amplifier.

The cascode current amplifiers also possess large bandwidth. This is because M_2 are nearly free of Miller effect. The Miller capacitances of M_2 are given by $C_{m1} = C_{gd2}(1 + \frac{g_{m3}}{g_{m2}})$ at the gate and $C_{m2} = C_{gd2}(1 + \frac{g_{m2}}{g_{m3}})$ at the drain. M_3 is common-gate configured and is not subject to Miller effect. From the current transfer function

$$\frac{I_o(s)}{I_{in}(s)} = \frac{g_{m2}}{g_{m1}} \frac{1}{s^2\left(\frac{C_{gs12}C_{gs3}}{g_{m1}g_{m3}}\right) + s\left(\frac{C_{gs12}}{g_{m1}} + \frac{C_{gs3}}{g_{m3}}\right) + 1}, \tag{2.9}$$

we obtain the poles of the system

$$p_{1,2} = \frac{g_{m1}g_{m3}}{2C_{gs12}C_{gs3}}\left\{-\left(\frac{C_{gs12}}{g_{m1}}+\frac{C_{gs3}}{g_{m3}}\right)\pm\left(\frac{C_{gs12}}{g_{m1}}-\frac{C_{gs3}}{g_{m3}}\right)\right\}$$
$$= \begin{cases} -\frac{g_{m1}}{C_{gs12}} \\ -\frac{g_{m3}}{C_{gs3}} \end{cases} \tag{2.10}$$

The bandwidth of the cascode current amplifier is the same as that of the basic current amplifier.

The biasing voltage can be obtained from the cascode itself, as shown in Fig.2.2(b). The minimum supply voltage of the self-biased cascode current amplifier of Fig.2.2(b) is $2V_T + V_{sat}$, increased from $V_T + V_{sat}$ of the externally biased cascode current amplifier of Fig.2.2(a).

Wilson current amplifier shown in Fig.2.2(c) [29] is another variation of cascode current amplifiers. The input impedance at low frequencies is given by $z_{in} = \frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}g_{m3}}$. The output impedance of Wilson current amplifier is given by $z_o \approx \left(\frac{g_{m1}g_{m3}}{g_{m2}}\right) r_{o3}r_{o1}$, the same output impedance as that of the basic cascode current amplifier. The current gain of Wilson current amplifier is given by

$$\frac{I_o(s)}{I_{in}(s)} = \frac{g_{m2}g_{m3}}{C_{gs12}C_{gs3}} \frac{s\left(\frac{C_{gs12}}{g_{m2}}\right)+1}{s^2 + s\left(\frac{g_{m1}+g_{m3}}{C_{gs12}}\right) + \frac{g_{m1}g_{m3}}{C_{gs12}C_{gs3}}}. \tag{2.11}$$

The current gain in the dc steady-state is the same as that of the basic cascode current amplifier. The zero is located at frequency $z = -\frac{g_{m2}}{C_{gs12}}$ and the complex conjugate poles are given by $p_{1,2} \approx \frac{g_{m1}}{C_{gs12}}(-1 \pm j)$ when $M_{1\sim3}$ are identical, resulting in $g_{m1} \approx g_{m3}$, $C_{gs12} = C_{gs1} + C_{gs2} \approx 2C_{gs3}$. Its bandwidth is the same as that of the basic current amplifier. Difficulties exist in obtaining an appropriate dc operating point of Wilson current amplifier because of the constraint $v_{DS1} > 2V_T$. This difficulty can be removed by adding another transistor in the input branch, as shown in Fig.2.2(d) [13]. Both the input and output impedances of the improved Wilson current amplifier can be obtained following a similar approach as that for Wilson current amplifier and the results are given by $z_{in} \approx \frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}g_{m4}}$ and $z_o \approx (g_{m1}r_{o1})r_{o4}$.

2.2.2 Regulated and Multi-Regulated Cascodes

To further increase the output impedance, a negative voltage-voltage feedback amplifier can be employed, as shown in Fig.2.3(a). The amplifier stabilizes the output current i_o when v_o varies. The auxiliary

amplifier can be implemented in various ways. Fig.2.3(b) is an implementation using a common-source amplifier [30].

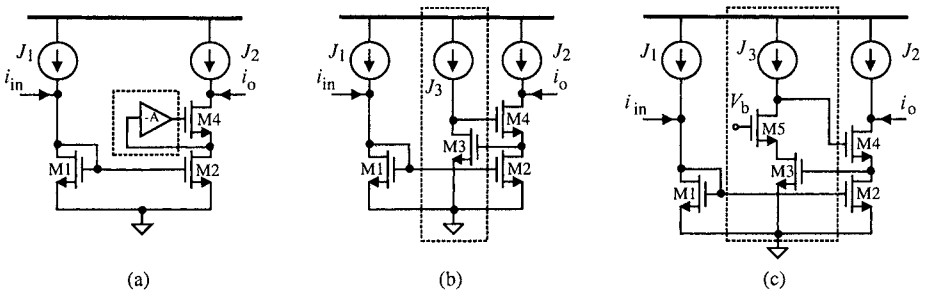

Figure 2.3. (a,b) Regulated cascode current amplifiers; (c) Multi-regulated cascode current amplifiers.

The output impedance of the regulated cascode current amplifier of Fig.2.3(a) can be derived from its small-signal equivalent circuit

$$\begin{aligned} r_o &= \frac{v_2}{i_T} = r_{o2}r_{o4}\Big[\frac{1}{r_{o2}} + \frac{1}{r_{o4}} + r_{o3}g_{m3}g_{m4} + g_{m3}\Big] \\ &\approx A(g_{m4}r_{o4})r_{o2}, \end{aligned} \tag{2.12}$$

where $A = g_{m3}r_{o3}$ the voltage gain of the auxiliary amplifier.

The output impedance can be further increased by boosting the voltage gain of the auxiliary amplifier. One approach is shown in Fig.2.3(c) where the feedback network itself is now a cascode amplifier. Replacing the term associated with the common-source auxiliary amplifier in (2.12) with the gain of the cascode amplifier given by $A_v = -(g_{m3}r_{o3})(g_{m5}r_{o5})$, we obtain the output impedance of the multi-regulated cascode current amplifier

$$r_o \approx \Big[(g_{m3}r_{o3})(g_{m5}r_{o5})\Big](g_{m4}r_{o4})r_{o2}. \tag{2.13}$$

It should be noted that the minimum supply voltage of the regulated and multi-regulated cascode current amplifiers is given by $2V_T + V_{sat}$, whereas that of the basic cascode current amplifiers is only $V_T + V_{sat}$.

2.2.3 Pseudo-Cascodes

Regulated and multi-regulated cascodes increase the output impedance, however, at the cost of a higher supply voltage. This is because in order to have a large output impedance, the biasing current source J_2 in

the output branch of the regulated and multi-regulated cascode current amplifiers must also be cascode-configured. To keep the supply voltage low and at the same time to ensure a large output impedance, the pseudo-cascode technique shown in Fig.2.4 was proposed in [27].

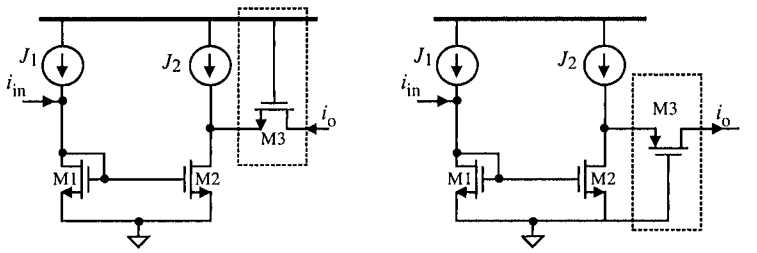

Figure 2.4. Pseudo-cascode current amplifiers.

Note that in this case, J_2 does not need to be implemented in cascode. The minimum supply voltage of the output branch is only $V_T + V_{sat}$. It can be shown that the output impedance of the pseudo-cascode current amplifiers is given by $z_o \approx (g_{m3} r_{o3}) r_{o2}$. The added common-gate stage has no negative effect on the bandwidth. Pseudo-cascodes are self-biased, making them attractive for low-power applications.

2.2.4 Low-Voltage Cascodes

Because V_T is usually much larger than V_{sat}, the cascode current amplifier of Fig.2.2(b) can be modified to Fig.2.5(a) to lower the supply voltage requirement while preserving the properties of the cascode current amplifiers. The minimum supply voltage of the low-voltage cascode current amplifier is given by $V_{DD,min} = V_T + V_{sat}$. The input impedance at low frequencies is given by $1/g_{m1}$, which is the same as that of the basic current amplifier. The output branch is the same as the basic cascode current amplifier with $z_o \approx (g_{m4} r_{o4}) r_{o2}$. To derive the current gain and bandwidth. Writing KCL at the gate and drain of M_1, the drain of M_2, and noting that $I_{in} = sC_{gs12}V_2 + g_{m3}(0 - V_1)$ and $I_o = g_{m4}(0 - V_3)$, we arrive at

$$\frac{I_o(s)}{I_{in}(s)} = \frac{g_{m2}}{g_{m1}} \frac{s\frac{C_{gs3}}{g_{m3}} + 1}{s^2 \frac{C_{gs3} C_{gs12}}{g_{m1} g_{m3}} + s\frac{C_{gs12}}{g_{m1}} + 1}. \tag{2.14}$$

The two poles are at

$$p_{1,2} = \frac{g_{m3}}{2C_{gs3}}\left[-1 \pm \sqrt{1 - 4\left(\frac{g_{m1}}{g_{m3}}\right)\left(\frac{C_{gs3}}{C_{gs12}}\right)}\right]. \tag{2.15}$$

If all transistors are of the same size, we arrive at $C_{gs12} \approx 2C_{gs3}$ and $g_{m1} \approx g_{m3}$. As a result, the poles become $p_{1,2} = \frac{g_{m1}}{C_{gs12}}(-1 \pm j)$. It is evident that the low-voltage cascode current amplifier has the same bandwidth as that of the basic cascode current amplifier.

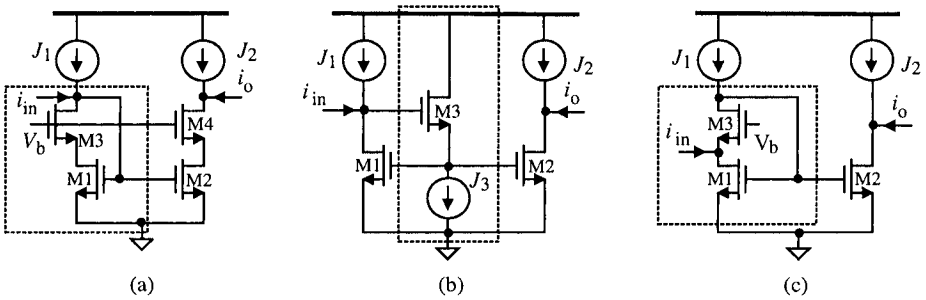

Figure 2.5. (a) Low-voltage cascode current amplifier; (b) Low input-capacitance current amplifier; (c) Low input impedance current amplifier.

2.3 Input-Impedance Reduction Techniques

Equally important as a large output impedance for current-mode circuits is a small input impedance. This is because a low input impedance reduces the loading-induced current error [31]. Also, in applications such as data links over wire channels, a low input impedance of the receivers is critical to increase the pole frequency at the input as the channels often have a large capacitance. This section investigates the techniques that reduce the input impedance of current-mode circuits.

2.3.1 Input-Capacitance Reduction

The capacitance seen from the input of the basic current amplifier is approximately $C_{in} \approx C_{gs1} + C_{gs2}$. To lower the input capacitance, a source follower can be employed at the input to isolate the gate capacitance $C_{gs1} + C_{gs2}$ from the input node, as shown in Fig.2.5(b) [32]. Because the Miller capacitances of M_3 are approximately zero, $C_{in} \approx 0$ holds. The input impedance at low frequencies is given by $z_{in} \approx \frac{1}{g_{m1}}$. The current gain at low frequencies is given by $\frac{i_o}{i_{in}} = \frac{g_{m2}}{g_{m1}}$, the same as that of the basic current amplifier.

2.3.2 Active Feedback

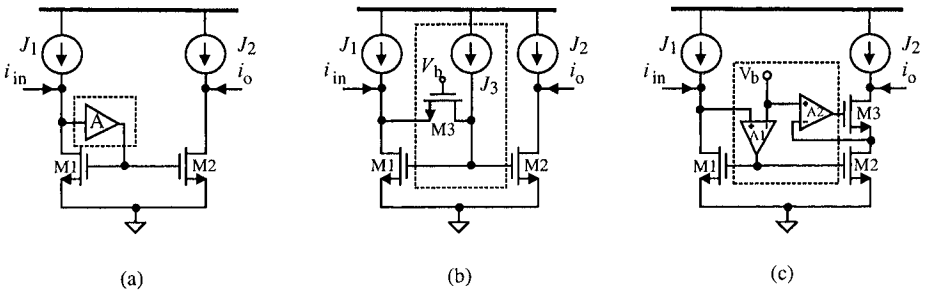

Figure 2.6. (a,b) Current amplifiers with input active feedback. (c) Current amplifiers with input active feedback and regulated cascode output.

Fig.2.6 make use of input active feedback to lower the input impedance. It is trivial to show that the input impedance of Fig.2.6(a) at low frequencies is given by $z_{in} \approx \frac{1}{Ag_{m1}}$, where A is the voltage gain of the auxiliary amplifier [33]. The auxiliary amplifier can be implemented in various ways provided that these implementations offer large bandwidth. In Fig.2.6(b), a common-gate configuration is employed to take the advantage of their immunity from Miller effect. Note that due to the close interaction with the feedback network, the input impedance of the current amplifier of Fig.2.6(b) increases rapidly at high frequencies when the effect of C_{gs}, C_{gd}, and parasitic junction capacitances are accounted for [34].

Both the active input feedback and regulated cascode can be employed simultaneously to lower the input impedance and boost the output impedance, as shown in Fig.2.6(c) [35]. It is readily to verify that the input impedance and output impedance of the active-input regulated-cascode current amplifier are given by $z_{in} \approx \frac{1}{A_1 g_{m1}}$ and $z_o \approx A_2(g_{m3}r_{o3})r_{o2}$.

The current amplifier shown in Fig.2.5(c) is another approach to implement the active feedback at the input. M_3 introduces a negative feedback to stabilize the input voltage, lowering the input impedance. The input impedance is given by $z_{in} = \frac{1}{(g_{m3}r_{o3})g_{m1}}$. Note that the minimum supply voltage requirement of the current amplifier is $V_T + V_{sat}$, the same as that of the basic current amplifier.

2.3.3 Bootstrapping

Basic cascode and regulated cascode current amplifiers are not particularly attractive for low-voltage design because in order to have a large output impedance, the biasing current source J_2 in the output branch

must also be cascode-configured. To achieve a low input impedance, a large output impedance, and at the same time to keep the supply voltage low, bootstrapped current amplifiers were proposed in [36]. The basic configuration of bootstrapped current amplifiers is shown in Fig.2.7(a). The auxiliary amplifier is employed to enable the input and output voltages to track each other. In addition, it lowers the input impedance and boosts the output impedance. The small-signal equivalent circuit of the bootstrapped current amplifier at low frequencies is shown in Fig.2.7(b). The output impedance is obtained form

$$z_o = \frac{v_2}{i_T} = \frac{g_{o1} + Ag_{m1}}{g_{o1}g_{o2} + A(g_{m1}g_{o2} - g_{m2}g_{o1})}. \tag{2.16}$$

Assume M_1 and M_2 are identical and $v_{DS1} = v_{DS2}$. This leads to $g_{m1}g_{o2} = g_{m2}g_{o1}$. Further because $g_{m1} \gg g_{o1}$, Eq.(2.16) is simplified to

$$z_o \approx A(g_{m1}r_{o1})r_{o2}. \tag{2.17}$$

Eq.(2.17) shows that the output impedance of the bootstrapped current amplifier is comparable to that of the regulated cascode current amplifier. It should be noted that J_2 must also be bootstrap-configured in order to have a large output impedance. The input impedance can be obtained in a similar manner and is given by $z_{in} \approx \frac{1}{Ag_{m1}}$.

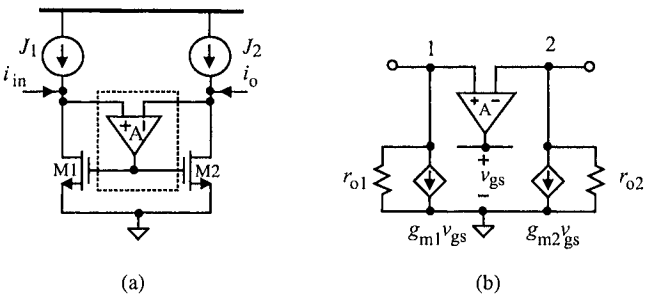

Figure 2.7. (a) Bootstrapped current amplifiers; (b) Small-signal equivalent circuit.

2.4 Mismatch Compensation Techniques

The basic current amplifiers suffer from device mismatches, mainly W/L- mismatch, V_T-mismatch, v_{GS}-mismatch, and v_{DS} mismatches. W/L-mismatch is due to the variation of fabrication processes. The dimension mismatch of transistors with multi-finger configuration differs from that of transistors with single-finger configuration, as shown in

Fig.2.8. In a 2-finger configuration case, $\Delta W = 2(\Delta W_1 + \Delta W_2)$ whereas in the one-finger configuration $\Delta W = \Delta W_1 + \Delta W_2$. For amplifiers with a current gain of A, we have

$$\left(\frac{W}{L}\right)_2 = A\left[\frac{W}{L} + \Delta\left(\frac{W}{L}\right)\right]. \tag{2.18}$$

Because

$$i_{D2} = \frac{(W/L)_2}{(W/L)_1}\left(\frac{v_{GS2} - V_{T2}}{v_{GS1} - V_{T1}}\right)^2\left(\frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}}\right) i_{D1}, \tag{2.19}$$

we arrive at

$$i_{D2} = A(1 + \delta_{W/L}) i_{D1}, \tag{2.20}$$

where $\delta_{W/L} = \frac{\Delta(W/L)}{W/L}$. The second term in (2.20) is the output offset current due to W/L-mismatch. v_{GS}-mismatch is mainly due to unbalanced interconnects connecting the gate and source of the input and output transistors. Let $v_{GS1} = v_{GS}$, $v_{GS2} = v_{GS} + \Delta v_{GS}$. Neglecting the second-order term in (2.19), we arrive at

$$i_{D2} = A(1 + \delta_{v_{GS}}) i_{D1}, \tag{2.21}$$

where $\delta_{v_{GS}} \approx \frac{2\Delta v_{GS}}{v_{GS} - V_T}$. Note that since the effective gate voltage $v_{GS} - V_T$ is usually small, $\delta_{v_{GS}}$ contributes significantly to the overall output offset current. V_T-mismatch is process-induced and can be analyzed in a similar way as v_{GS}-mismatch.

$$i_{D2} = A(1 + \delta_{V_T}) i_{D1}, \tag{2.22}$$

where $\delta_{V_T} \approx -\frac{2\Delta V_T}{v_{GS} - V_T}$. For the same reason as that for v_{GS}-mismatch, V_T-mismatch is critical. In a similar manner as that of v_{GS}-mismatch, one can analyze the effect of v_{DS}-mismatch

$$i_{D2} = A(1 + \delta_{v_{DS}}) i_{D1}, \tag{2.23}$$

where $\delta_{v_{DS}} = \frac{\lambda \Delta v_{DS}}{1 + \lambda v_{DS}}$.

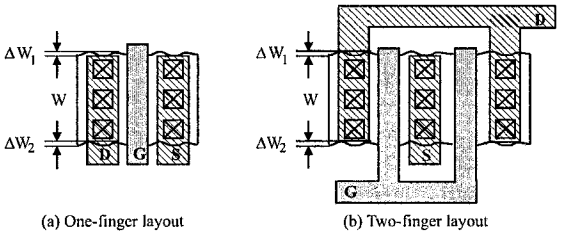

Figure 2.8. Dimension mismatch of multi-finger transistors.

For practical circuits, since $v_{gs} \ll V_{GS}$, $v_{ds} \ll V_{DS}$, we have $\Delta v_{gs} \ll \Delta V_{GS}$ and $\Delta v_{ds} \ll \Delta V_{DS}$, subsequently $\Delta v_{GS} \approx \Delta V_{GS}$ and $\Delta v_{DS} \approx \Delta V_{DS}$. This leads to $\delta_{v_{GS}} \approx \frac{2\Delta V_{GS}}{V_{GS}-V_T}$, $\delta_{V_T} \approx -\frac{2\Delta V_T}{V_{GS}-V_T}$, and $\delta_{v_{DS}} \approx \frac{\lambda \Delta V_{DS}}{1+\lambda V_{DS}}$. Because $i_{D1} = i_{in} + J$, the output current of the current amplifier with mismatches considered is given by

$$\begin{aligned} i_o &= A(1+\delta)(i_{in}+J) \\ &= A(i_{in}+J) + \delta A(i_{in}+J), \end{aligned} \tag{2.24}$$

where the mismatch coefficient δ in the worst case is obtained from

$$\delta = |\delta_{W/L}| + |\delta_{V_{GS}}| + |\delta_{V_T}| + |\delta_{V_{DS}}|. \tag{2.25}$$

The second term on the right hand side of (2.24) is the mismatch-induced output offset current and is denoted by i_{os}. It consists of two components : the signal-dependent component $i_{os1} = \delta A i_{in}$ and the bias-dependent component $i_{os2} = \delta A J$. i_{os2} can be removed by employing a two-phase clock that samples and holds the offset current in one clock phase and substrates the held offset current from the output current of the current amplifiers in the following clock phase [37–39].

Because i_{os2} is time-invariant, it can also be compensated effectively using the balancing network shown in Fig.2.9 [40, 41]. To simplify analysis, we assume that all nMOS current mirrors have the same mismatch coefficient δ_n and all pMOS current mirrors have the same mismatch coefficient δ_p. Making use of (2.24)

$$i_{D2} = A_1(i_{in}+J) + \delta_n A_1(i_{in}+J), \tag{2.26}$$

and

$$i_{D4} = A_2\Big[A_1(i_{in}+J) + \delta_n A_1(i_{in}+J)\Big]$$

$$\begin{aligned} &+ \quad \delta_p A_2\Big[A_1(i_{in}+J)+\delta_n A_1(i_{in}+J)\Big] \\ \approx \quad & A_1A_2i_{in}+A_1A_2J+A_1A_2\delta_n i_{in} \\ &+ \quad A_1A_2\delta_n J+A_1A_2\delta_p i_{in}+A_1A_2\delta_p J, \end{aligned} \tag{2.27}$$

where 2nd-order terms were neglected. In a similar manner one can shown

$$i_{D5}\approx A_1A_2J+A_1A_2\delta_p J+A_1A_2\delta_n J. \tag{2.28}$$

The subtraction of (2.28) from (2.27) yields

$$i_o \quad = A_1A_2i_{in}+A_1A_2(\delta_n+\delta_p)i_{in}. \tag{2.29}$$

It is seen from (2.29) that the output offset current is reduced from $A_1A_2(\delta_n+\delta_p)J+A_1A_2(\delta_n+\delta_p)i_{in}$ without the balancing network to $A_1A_2(\delta_n+\delta_p)i_{in}$ with it. Figs.2.10 and 2.11 compare the Monte Carlo simulation results of the output current with and without the balancing network. It should be noted that the balancing network approach consumes additional power and silicon area.

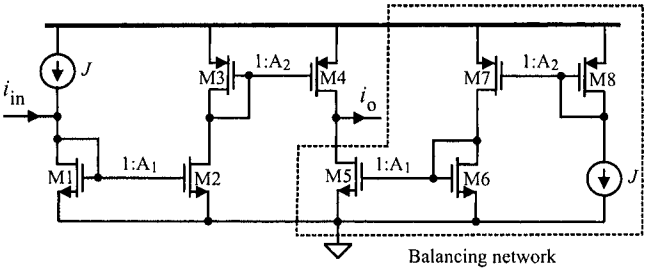

Figure 2.9. Balancing network for mismatch compensation of current amplifiers.

2.5 Power Reduction Techniques

One of the drawbacks of current-mirror amplifiers is their high static power consumption, arising mainly from the large biasing current of the output branch. Consider the two-stage current amplifier shown in Fig.2.12 with $J_c = 0$. The output current is given by $i_o = A_1A_2i_{in}$ and the biasing current of the output branch is given by $J_2 = A_1A_2J_1$. Since the purpose of the second stage is to amplify i_{d2}, not I_{D2}, this suggests that I_{D3} should be kept small. To achieve this, the dc current source $J_c = A_cJ_1$, as shown in Fig.2.12, is added [42, 28]. The channel

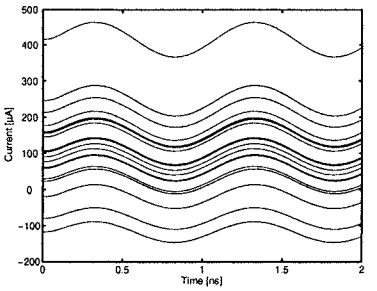

Figure 2.10. Simulated output current without the balancing network (Standard deviation of dimension=10%, 20 samples).

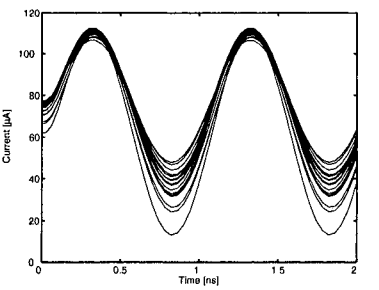

Figure 2.11. Simulated output current with the balancing network (Standard deviation of dimension=10%, 20 samples).

current of M_2 is given by $i_{D2} = A_1(i_{in} + J_1)$ and that of M_3 is given by $i_{D3} = A_1 i_{in} + (A_1 - A_c)J_1$. If we impose $A_1 - A_c = 1$ and $J_2 = A_2 J_1$, the output current is given by $i_o = A_1 A_2 i_{in}$. In addition to the power consumption reduction, the chip area is also reduced due to smaller M_3 and M_4. This is echoed with an increase in the bandwidth, as is evident in Fig.2.13.

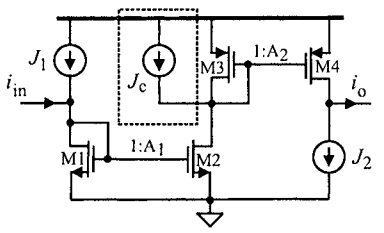

Figure 2.12. Current-branching.

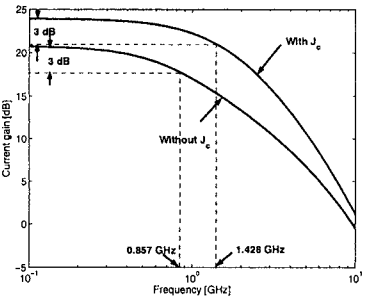

Figure 2.13. Simulated bandwidth of amplifier with current-branching. The amplifier is implemented in TSMC-0.18μm CMOS technology.

2.6 Bandwidth Enhancement Techniques

Resistor series peaking, inductor series peaking, and current feedback are three effective means to improve the bandwidth of current-mode circuits. This section examines these techniques.

2.6.1 Resistor Series Peaking

It was shown in [43, 44] that a resistor can be added between the gates of the input and output transistors of the basic current amplifier, as shown in Fig.2.14, to introduce a zero to the system. The current transfer function is given by

$$H(s) = \left(\frac{g_{m2}}{g_{m1}}\right) \frac{sRC_{gs1} + 1}{s^2 \frac{RC_{gs1}C_{gs2}}{g_{m1}} + s\frac{C_{gs1}+C_{gs2}}{g_{m1}} + 1}. \tag{2.30}$$

The two poles are at

$$p_{1,2} = \frac{C_{gs1} + C_{gs2}}{2RC_{gs1}C_{gs2}} \left[-1 \pm \sqrt{1 - \frac{4RC_{gs1}C_{gs2}g_{m1}}{(C_{gs1} + C_{gs2})^2}} \right], \tag{2.31}$$

and the zero is at $z = -\frac{1}{RC_{gs1}}$. Depending upon the value of the peaking resistor R, the locations of both the zero and poles of the system differ and the amplifier exhibits distinct characteristics. (1) *Distinct real poles* - When $R = \frac{1}{g_{m1}}$, the amplifier has two distinct negative real poles located at $p_1 = -\frac{g_{m1}}{C_{gs2}}$ and $p_2 = -\frac{g_{m1}}{C_{gs1}}$. Observe that p_2 is identical to the zero given by $z = -\frac{g_{m1}}{C_{gs1}}$ and cancels out the zero. As a result, the transfer function is simplified to

$$H(s) = \left(\frac{g_{m2}}{g_{m1}}\right) \frac{1}{s\frac{C_{gs2}}{g_{m1}} + 1}. \tag{2.32}$$

As compared with the bandwidth of the basic current amplifier, the resistor series peaking with two distinct real poles boosts the bandwidth to $\omega_b = \frac{g_{m1}}{C_{gs2}}$. Note that if $C_{gs2} \gg C_{gs1}$, the bandwidth improvement from resistive series peaking with two distinct real poles is rather small. (2) *Identical real poles* - When $R = \frac{1}{4g_{m1}} \frac{(C_{gs1}+C_{gs2})^2}{C_{gs1}C_{gs2}} \approx \frac{1}{4g_{m1}} \frac{C_{gs2}}{C_{gs1}}$, the circuit has two identical negative real poles $p_{1,2} = -\frac{2g_{m1}}{C_{gs1}+C_{gs2}}$. The bandwidth becomes $\omega_b = 2\sqrt{\sqrt{2}-1}\frac{g_{m1}}{C_{gs2}}$. (3) *Complex conjugate poles* - A further increase of R will lead to a pair of complex conjugate poles. An overshoot in the frequency-domain response and ringing in the time-domain response exist. A critical point is when $R = \frac{1}{2g_{m1}} \frac{C_{gs2}}{C_{gs1}}$. The amplifier has two complex conjugate poles that are separated by $\frac{\pi}{2}$ and has a maximally flat response, called Butterworth response, with the bandwidth given by $\omega_b = \sqrt{2}\frac{g_{m1}}{C_{gs2}}$ [45]. In this case, the time-domain response of the

amplifier to a unit-step input has an overshoot of 4.32% approximately [46]. Fig.2.15 shows the dependence of the bandwidth of the current amplifier with the resistor series peaking on the resistance of the peaking resistor.

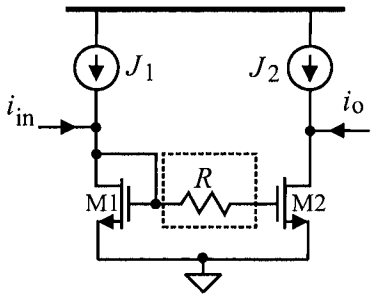

Figure 2.14. Basic current amplifier with resistor series peaking.

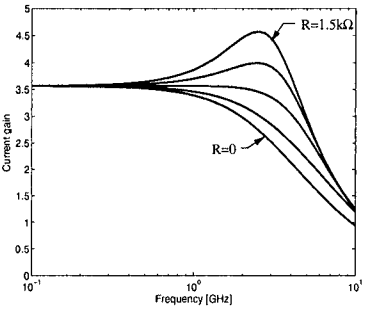

Figure 2.15. Simulated frequency response of current amplifier with resistor series peaking. R is varied from 0 to 1.5 $k\Omega$ with step 0.375 kΩ. The amplifier is implemented in TSMC-0.18μm CMOS technology.

2.6.2 Inductor Series Peaking

The thermal noise of the series peaking resistor increases the total noise of the amplifier. For low-noise applications, such as the front-end of Gb/s transceivers and optical pre-amplifiers, noiseless elements, such as inductors, are preferred over noisy resistors for bandwidth enhancement. It has been demonstrated that inductor shunt peaking can increase the bandwidth of voltage-mode circuits by as much as 70% [47, 48]. Inductor shunt-peaking technique, however, is not particularly applicable to current-mode circuits due to the existence of biasing current sources between the devices forming the dominant poles and the supply voltage. The fact that the dominant pole of the basic current amplifier is located at the gates of M_1 and M_2 suggests that an inductor can be placed between the gates of M_1 and M_2, as shown in Fig.2.16, to boost bandwidth. By assuming $C_{gs2} \gg C_{gs1}$, we obtain the current transfer function

$$\frac{I_o(s)}{I_{in}(s)} = \left(\frac{g_{m2}}{g_{m1}}\right) \frac{1}{s^2 L C_{gs2} + s\frac{C_{gs2}}{g_{m1}} + 1}. \tag{2.33}$$

The two poles are located at

$$p_{1,2} = \frac{1}{2Lg_{m1}}\left(-1 \pm \sqrt{1 - \frac{4Lg_{m1}^2}{C_{gs2}}}\right). \tag{2.34}$$

Under the condition $L = \frac{C_{gs2}}{4g_{m1}^2}$, the amplifier has two identical real poles $p_{1,2} = -\frac{2g_{m1}}{C_{gs2}}$. Its time response is critically damped with no ringing. The bandwidth in this case is given by $\omega_b = 2\sqrt{\sqrt{2}-1}\left(\frac{g_{m1}}{C_{gs2}}\right)$. When L is increased to $L = \frac{C_{gs2}}{2g_{m1}^2}$, the amplifier has two complex conjugate poles that are separated by $\frac{\pi}{2}$. In this case, the response of the amplifier has a maximally flat (Butterworth) passband with the bandwidth given by $\omega_b = \sqrt{2}\left(\frac{g_{m1}}{C_{gs2}}\right)$ [45]. Fig.2.17 shows the frequency response of the current amplifier with inductor series peaking. The attenuation rate of the response in the stop band, which is approximately -40 dB/decade, is higher as compared with that of the amplifier with resistive series peaking. This is because the former increases the bandwidth by adding a pole whereas the latter enhances the bandwidth by introducing a zero. The peaking inductor does not affect the dc characteristics of the amplifier, a similar property as that of the resistor series peaking.

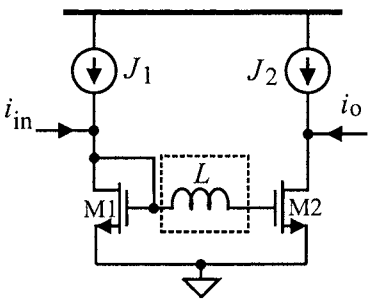

Figure 2.16. Inductor series peaking in current-mode circuits.

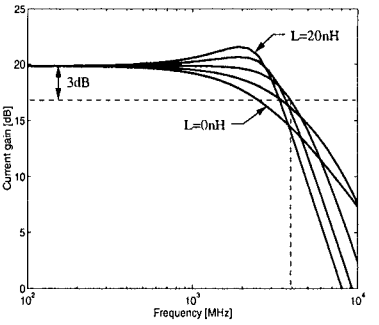

Figure 2.17. Simulated frequency response of current amplifier with inductor series peaking. The value of the series peaking inductor is varied from 0 to 20nH with step 5nH. The amplifier is implemented in TSMC-0.18μm CMOS technology.

On-chip inductors are usually implemented in either planar or stacked spiral configurations, as shown in Fig.2.18. Spiral inductors have the characteristics of a low quality factor, a low inductance, and extremely area-consuming [47–49]. The ohmic loss of spiral inductors, mainly due to the skin-effect induced loss at high frequencies, is usually depicted

using a series resistor R_s. Its capacitive loss, arising from the large capacitance between the spirals and the substrate, is represented by two shunt capacitors C_{ox} at the terminals of the inductor. The capacitive coupling between the upper and lower spirals at the under-paths and fringe capacitance between neighboring spirals is characterized by C_s, as shown in the simple lumped model of on-chip spiral inductors in Fig.2.19.

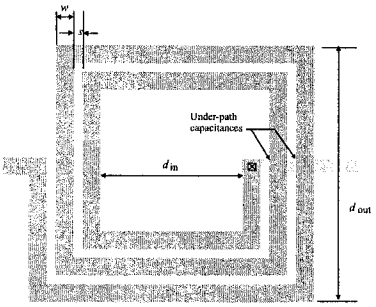

Figure 2.18. Typical layout of square-shaped spiral inductors.

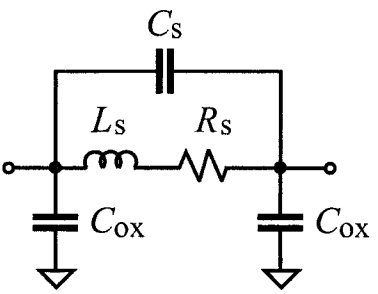

Figure 2.19. Simple lumped model of on-chip spiral inductors.

The series resistance of the inductor behaves as a series peaking resistor and improves the bandwidth, as shown in Fig.2.20. The spiral-substrate shunt capacitance, however, is directly added to the total capacitance of the gates of $M_{1\sim2}$ of the current amplifier, lowering the bandwidth, as evident in Fig.2.21.

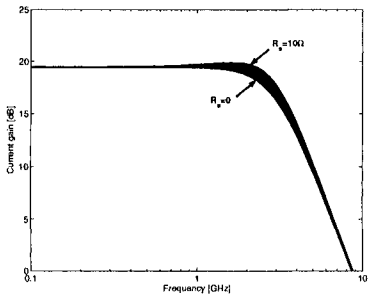

Figure 2.20. Simulated effect of the series resistance of series peaking inductors on the frequency response of the current amplifier implemented in TSMC-0.18μm CMOS technology.

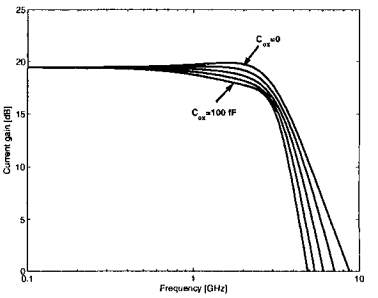

Figure 2.21. Simulated effect of the parasitic capacitance of series peaking inductors on the frequency response of the current amplifier implemented in TSMC-0.18μm CMOS technology.

2.6.3 Current Feedback

It is well known that negative current-current feedback increases the output impedance and lowers the input impedance [50, 51]. To sense the output current without affecting both the dc biasing condition and the supply voltage, the current feedback mechanism shown in Fig.2.22 can be used. The transfer function of the amplifier is given by

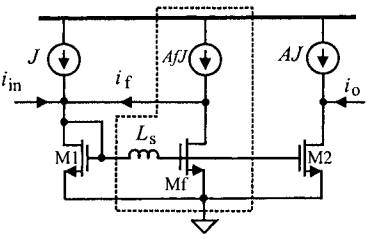

Figure 2.22. Current amplifier with both current-current feedback and inductor series peaking.

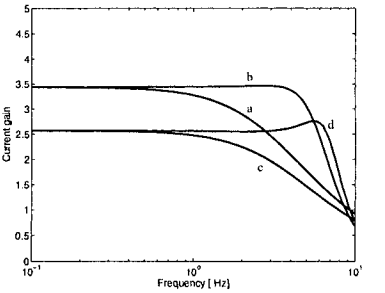

Figure 2.23. Simulated frequency response of current amplifiers with both current-current feedback and inductor series peaking. (a) Basic current amplifier; (b) Inductor series peaking only; (c) Current-current feedback; (d) Inductor series peaking and current-current feedback The amplifiers are implemented in TSMC-0.18μm CMOS technology.

$$H(s) \approx \left(\frac{g_{m2}}{g_{m1}}\right) \frac{\frac{1}{LC_{gs2}}}{s^2 + s\frac{1}{g_{m1}L} + \frac{g_{m1}+g_{mf}}{g_{m1}LC_{gs2}}}, \tag{2.35}$$

with two poles at

$$p_{1,2} = \frac{1}{2g_{m1}L}\left[-1 \pm \sqrt{1 - \frac{4(g_{m1}+g_{mf})g_{m1}L}{C_{gs2}}}\right]. \tag{2.36}$$

Complex conjugate poles that are $\frac{\pi}{2}$ apart occurs when $L = \frac{C_{gs2}}{2g_{m1}^2(1+Af)}$, where $A = \frac{(W/L)_2}{(W/L)_1}$ and $f = \frac{(W/L)_f}{(W/L)_2}$. In this case, the amplifier has a maximally flat response with the bandwidth $\omega_b = \sqrt{2}(1+Af)\frac{g_{m1}}{C_{gs2}}$. The value of the series peaking inductor that gives a maximally flat response is reduced from $L = \frac{C_{gs2}}{2g_{m1}^2}$ without the current-current feed-

back to $L = \frac{C_{gs2}}{2g_{m1}^2}\frac{1}{(1+Af)}$ with the current-current feedback. A smaller inductor, subsequently, a smaller chip area and less parasitic effects, is needed when current-current feedback is employed. Fig.2.23 shows the frequency response of the current amplifier with both inductor series peaking and current-current feedback.

In a similar manner, one can show that the amplifier with both resistor series peaking and current-current feedback, as shown in Fig.2.24, has the current transfer function

$$H(s) = \left(\frac{g_{m2}}{g_{m1}+g_{mf}}\right)\frac{sRC_{gs1}+1}{s^2\frac{RC_{gs1}(C_{gs2}+C_{gs,f})}{g_{m1}+g_{mf}} + s\frac{C_{gs1}+C_{gs2}+C_{gs,f}+RC_{gs1}g_{mf}}{g_{m1}+g_{mf}} + 1} \tag{2.37}$$

Assume $Rg_{mf} \ll 1$ and $C_{gs,f} \ll C_{gs1}, C_{gs2}$, we have two poles

$$p_{1,2} \approx \frac{C_{gs1}+C_{gs2}}{2RC_{gs1}C_{gs2}}\left[-1 \pm \sqrt{1-\frac{4RC_{gs1}C_{gs2}g_{m1}(1+Af)}{(C_{gs1}+C_{gs2})^2}}\right]. \tag{2.38}$$

When $R = \frac{1}{2g_{m1}}\frac{C_{gs2}}{C_{gs1}}\frac{1}{1+Af}$, the amplifier has a maximum plat response with its bandwidth $\omega_b = \sqrt{2}(1+Af)\frac{g_{m1}}{C_{gs2}}$. Also, the resistance value is reduced from $R = \frac{1}{2g_{m1}}\frac{C_{gs2}}{C_{gs1}}$ without the current-current feedback to $R = \frac{1}{2g_{m1}}\frac{C_{gs2}}{C_{gs1}}\frac{1}{1+Af}$ with the current-current feedback. Fig.2.25 shows the current gain of the amplifiers with the resistor series peaking and current-current feedback.

2.7 Dynamic Range Improvement Techniques

The application of class-A current amplifiers is limited by the small current swing because a large current swing would require the quiescent point to be far away from the pinch-off, resulting in a large drain-source voltage. To accommodate high-current applications, class AB configurations that employ a pair of nMOS and pMOS current mirrors activated separately are effective, as shown in. Fig.2.26 [40]. Transistors $M_{11\sim12}$ provide a low input impedance. When a large positive input current is applied at the input (the current flows into the channel), the voltage of the input node arises sufficiently high such that the pMOS current mirror is disabled. The input current is sensed by the nMOS current mirror. Similarly, when a large negative current is applied to the input (the current flows away from the channel), the low voltage at the input

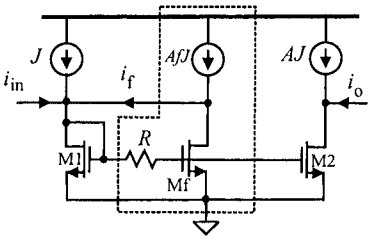

Figure 2.24. Current amplifier with both current-current feedback and resistor series peaking.

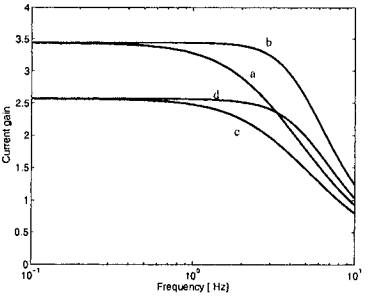

Figure 2.25. Simulated frequency response of current amplifiers with both current-current feedback and resistor series peaking. (a) Basic current amplifier; (b) Resistor series peaking; (c) Current-current feedback; (d) Resistor series peaking and current-current feedback. The amplifiers are implemented in TSMC-0.18μm CMOS technology.

node forces M_{11} enter the cut-off mode and the current flowing out of the input node is sourced by the pMOS current mirror. It should, however, be noted that when the amplitude of the input current is small, both the nMOS and pMOS current mirrors are activated, giving rise to static power consumption. The dc operating point of the class AB current amplifier is set to such that $V_{in} = V_{DD}/2$ and the minimum supply voltage is given by $V_{DD,min} = 2V_T + 2V_{sat}$.

The low-voltage class AB current amplifier shown in Fig.2.26(b) lowers the minimum supply voltage to $2V_T$ [52]. The main drawback of this current amplifier is that the quiescent currents are strongly influenced by both the threshold and supply voltages. To minimize the effect of a finite output impedance of the preceding class AB current amplifier, cascode configuration can be employed at both the output stages, as shown in Fig.2.26(c) [53]. The output impedance at low frequencies is given by $r_o \approx (g_{m13}r_{o13})r_{o8}||(g_{m14}r_{o14})r_{o10}$. In [54], a bootstrapped cascode class AB current amplifier shown in Fig.2.26(d), was proposed [54]. The bootstrapped configuration boosts the output impedance to $r_o = A(g_{m3}r_{o3})r_{o6}||A(g_{m4}r_{o4})r_{o8}$. The added auxiliary differential amplifiers also minimize the output error current of current mirrors $M_{5\sim6}$ and $M_{7\sim8}$ due to v_{DS}-mismatch.

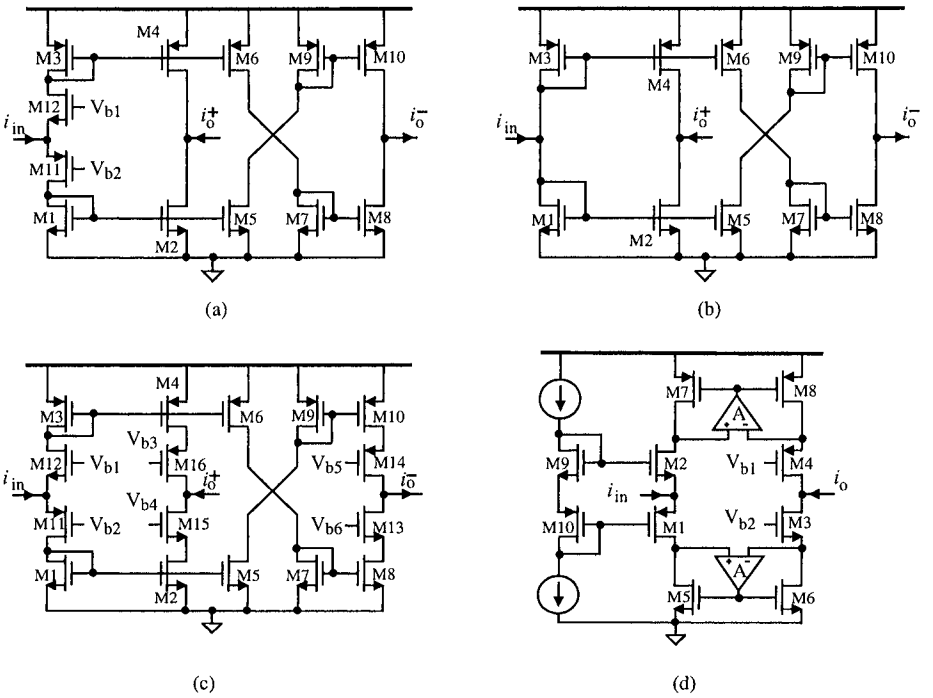

Figure 2.26. (a) Basic class AB current amplifiers; (b) Low-voltage class AB current amplifiers; (c) Cascode class AB current amplifiers; (d) Bootstrapped Class AB current amplifiers.

2.8 Active Inductors

CMOS spiral inductors suffer from a number of drawbacks intrinsic to the spiral layout of the inductors and CMOS technologies including a low quality factor, a low self-resonant frequency, a small and non-tunable inductance, and require a prohibitively large chip-area [49, 55, 56, 47]. Active inductors offer many unique advantages over their spiral passive counterparts including virtually no chip area requirement, a large and tunable inductance, a high quality factor, and fully compatible with standard CMOS technologies [57–70]. These inductors have been used successfully in many applications where inductors are required, as demonstrated in Table 2.1. The effectiveness of active inductors, however, is affected by a number of limitations including a small dynamic range, a high noise level, high power consumption, and a finite useful frequency range.

Table 2.1. Applications of active inductors.

Application	Technology	Reference
SONET OC-48 optical receivers with bandwidth 3GHz	0.25μm	[61]
2.5 Gbps optical front-ends	0.35μm	[68]
VCOs for 4 Gbps CDR	0.25μm	[69]
5GHz VCOs (-81dBc/Hz phase noise at 500kHz offset)	0.20μm	[71]
Low-pass with 4.57GHz cut-off frequency	0.18μm	[72]
RF band-pass filter ($f_o = 900$MHz, $Q = 41$)	0.35μm	[63–65]
1GHz LNA (NF=2-3dB)	0.5μm	[73]
2.4GHz LNA (NF=2dB)	0.3μm	[74]

2.8.1 Topologies of Active Inductors

Gyrator-C Active Inductors

Gyrators are two back-to-back connected transconductors. When one port is terminated with a capacitive load, as shown in Fig.2.27, the other port exhibits an inductive characteristic [67]. In the ideal case where the input impedance of the transconductors is infinite, the admittance looking into port 1 of the gyrator is given by

$$Y(s) = sC_2 + G_{o2} + \frac{1}{s\left(\frac{C_1}{g_{m1}g_{m2}}\right) + \frac{G_{o1}}{g_{m1}g_{m2}}}. \tag{2.39}$$

Eq.(2.39) can be represented equivalently by the RLC network shown in Fig.2.27 with $R_p = \frac{1}{G_{o2}}$, $C_p = C_2$, $R_s = \frac{G_{o1}}{g_{m1}g_{m2}}$, and $L = \frac{C_1}{g_{m1}g_{m2}}$. If $G_{o1,2} = 0$ and $C_2 = 0$, we have $R_s = 0$, $R_p = \infty$, and $C_p = 0$. Port 1 of the gyrator behaves as a lossless inductor.

To find out the effective frequency range over which the gyrator is inductive, we examine the impedance looking into the inductor

$$Z(s) = \left(\frac{R_s}{C_pL}\right)\frac{s\frac{L}{R_s} + 1}{s^2 + s\left(\frac{1}{R_pC_p} + \frac{R_s}{L}\right) + \frac{R_p+R_s}{R_pC_pL}}. \tag{2.40}$$

When complex conjugate poles are encountered, the impedance has its self-resonant frequency at $\omega_o \approx \sqrt{\frac{1}{LC_p}} = \sqrt{\omega_{t1}\omega_{t2}}$, where $R_p \gg R_s$ was utilized and $\omega_{t1,2} = \frac{g_{m1,2}}{C_{1,2}}$ is the cut-off frequency of the transconductors. Observe that $Z(s)$ has a zero at the frequency $\omega_z = \frac{R_s}{L} = \frac{G_{o1}}{C_1}$. The Bodé

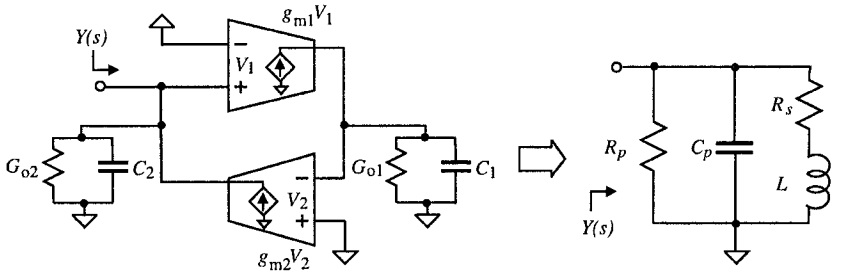

Figure 2.27. Grounded Gyrator-C active inductors.

plots of $Z(j\omega)$ are sketched in Fig.2.28. It is evident that the gyrator is resistive when $\omega < \omega_z$, inductive when $\omega_z < \omega < \omega_o$, and capacitive when $\omega > \omega_o$. Also, R_p has no effect on the frequency range of the active inductors, whereas R_s sets the lower frequency bound. To maximize the frequency range over which the gyrator is inductive, ω_z should be minimized and ω_o should be maximized.

The quality factor Q of the inductor quantifies the ratio of the net magnetic energy stored to the energy dissipated by the inductor in one oscillation cycle [55, 75]. It is obtained by examining the impedance of the active inductor in the sinusoidal steady state $Z(j\omega) = \Re e[Z(j\omega)] + j\Im m[Z(j\omega)]$

$$Q(\omega) = \frac{\Im m\left[Z(j\omega)\right]}{\Re e\left[Z(j\omega)\right]}. \tag{2.41}$$

From (2.40), we have

$$Q(\omega) = \left(\frac{\omega L}{R_s}\right) \frac{R_p}{R_p + R_s\left[1 + (\frac{\omega L}{R_s})^2\right]} \left[1 - \frac{R_s^2 C_p}{L} - \omega^2 L C_p\right]. \tag{2.42}$$

Fig.2.29 shows the frequency dependence of the quality factor. It is seen that the first term in (2.42), denoted by

$$Q_1(\omega) = \frac{\omega L}{R_s}, \tag{2.43}$$

quantifies the quality factor at low frequencies. The second term, denoted by

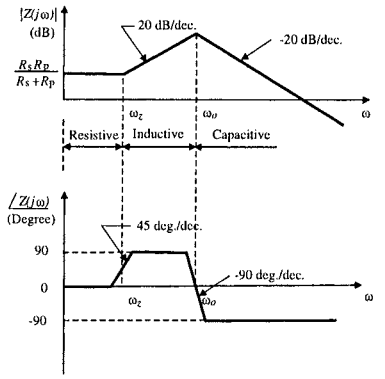

Figure 2.28. Sketch of the Bodé plots of gyrator-C active inductors.

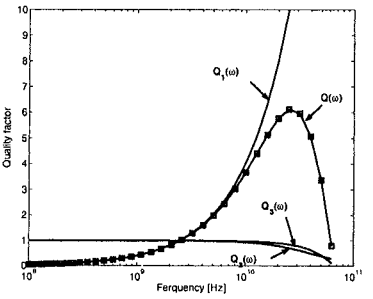

Figure 2.29. Quality factor ($R_s = 4\Omega$, $R_p = 1k\Omega$, $C_p = 140$ fF, and $L = 1.6$ nH [55])

$$Q_2(\omega) = \frac{R_p}{R_p + R_s\left[1 + (\frac{\omega L}{R_s})^2\right]}, \tag{2.44}$$

accounts for the effect of the finite output impedance of deep sub-micron MOSFETs, whereas the third term, denoted by

$$Q_3(\omega) = 1 - \frac{R_s^2 C_p}{L} - \omega^2 L C_p, \tag{2.45}$$

shows that the quality factor vanishes when frequency approaches the self-resonant frequency of the active inductor. $Q_2(\omega)$ and $Q_3(\omega)$ manifest their impact at high frequencies only. Because active inductors usually operate in the lower portion of the frequency range $\omega_z < \omega < \omega_o$, $Q_1 = \frac{\omega L}{R_s}$ is usually used to quantify the quality factor of the active inductors approximately.

The sensitivity of the quality factor with respect to R_p and R_s is investigated in Figs.2.30 and 2.31. It is seen that $Q(\omega)$ is sensitive to R_s at low frequencies, revealing that in order to boost $Q(\omega)$, minimizing R_s is essential. R_p, on the other hand, only affects $Q(\omega)$ at high frequencies. The increase of ω_o due to the increase of R_p and the decrease of ω_o due to the decrease of R_s are due to the 2nd-order effects and are marginal.

Gyrator-C active inductors with a high self-resonant frequency mandate the configuration of the transconductors be as simple as possible. Most gyrator-C active inductors employ common-source configuration as negative transconductors, common-gate and source follower config-

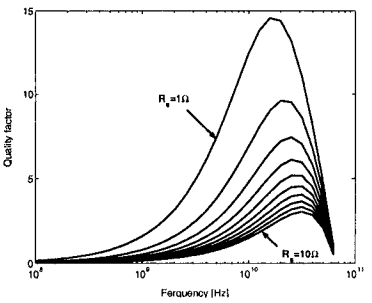

Figure 2.30. The effect of R_s on quality factor. R_s is varied from 1Ω to 10Ω with step 1Ω.

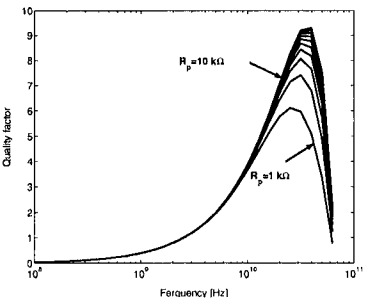

Figure 2.31. The effect of R_p on quality factor. R_p is varied from 1kΩ to 10kΩ with step 1kΩ.

urations as positive transconductors, as shown in Fig.2.32. The load capacitors C_1 and C_2 in Fig.2.27 are realized using the intrinsic capacitance C_{gs} of the devices to maximize the upper bound of the frequency range of inductors.

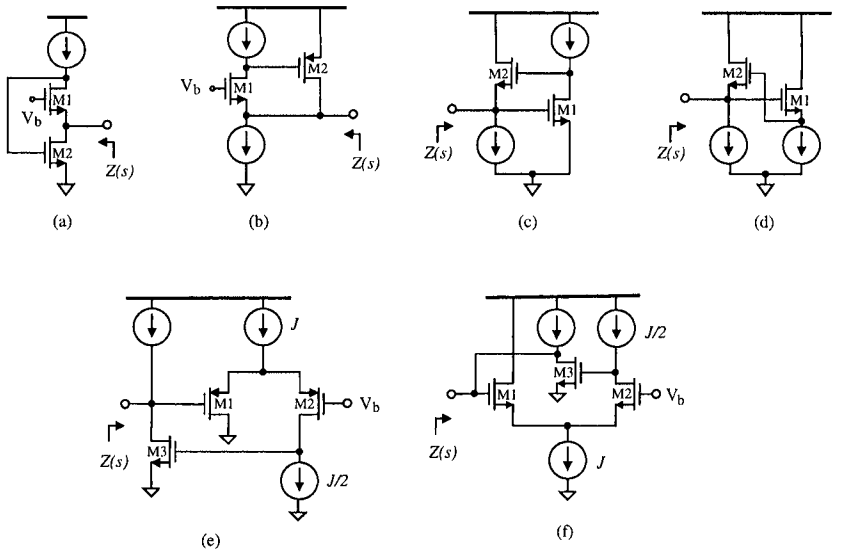

Figure 2.32. Typical configurations of grounded gyrator-C active inductors. (a) [63–66], (b)[59, 60], (c) [57], (d) [59, 60], (e) [76, 71], (f) [77].

It can be shown that when C_{gd} is neglected, the parameters of the equivalent RLC network of these active inductors are given by $C_p = C_{gs1}$, $R_p = \frac{1}{g_{m1}}$, $L = \frac{C_{gs2}}{g_{m1}g_{m2}}$, and $R_s = \frac{g_{o1}}{g_{m1}g_{m2}}$. The self-resonant

frequency of these active inductors is given by $\omega_o \approx \frac{1}{\sqrt{LC_p}} = \sqrt{\omega_{t1}\omega_{t2}}$ and the frequency of the zero is given by $\omega_z = \frac{g_{o1}}{C_{gs2}}$.

Cascode Gyrator-C Active Inductors

To maximize the effective frequency range of active inductors, ω_z should be minimized and ω_o should be maximized. Maximizing ω_o is rather difficult simply because ω_o of the active inductors approaches the cutoff frequency of the transconductors. $\omega_z = \frac{g_{o1}}{C_{gs2}}$, on the other hand, can be lowered effectively by either increasing C_{gs2} or decreasing g_{o1}. The former is at the cost of lowering ω_o and should therefore be avoided. To reduce g_{o1}, cascode as shown in Fig.2.33(b) is proven to be effective. The impedance of the cascode active inductor is given by

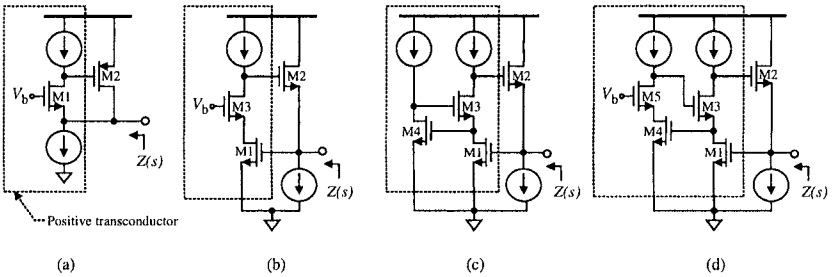

Figure 2.33. (a) gyrator-C, (b) cascode, (c) regulated cascode, (d) multi-regulated cascode gyrator-C active inductors. Cascodes are implemented in the positive transconductors to reduce g_{o1}.

$$Z(s) \approx \left(\frac{g_{o1}g_{o3}}{C_{gs1}C_{gs2}g_{m3}}\right) \frac{s\left(\frac{C_{gs2}g_{m3}}{g_{o1}g_{o3}}\right) + 1}{s^2 + s\left(\frac{g_{o1}g_{o3}}{C_{gs2}g_{m3}} + \frac{g_{o1}}{C_{gs1}}\right) + \frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}}, \qquad (2.46)$$

where $g_m \gg g_o$ was used to simplify results. The parameters of the RLC equivalent network of the cascode active inductor can be obtained by examining the admittance of the inductor and the results are given by $R_p = \frac{1}{g_{o2}}$, $C_p = C_{gs1}$, $R_s = \left(\frac{g_{o1}}{g_{m1}g_{m2}}\right)\frac{1}{g_{m3}r_{o3}}$, and $L = \frac{C_{gs2}}{g_{m1}g_{m2}}$. A comparison of the parameter of the gyrator-C and cascode gyrator-C active inductors is provided in Table 2.2. It is seen from the table that the use of cascode has the following positive impacts : (i) lowers the frequency of the zero and expends the frequency range over which an inductive characteristic exists, (ii) reduces the series resistance, (iii) increases the parallel resistance, and (iv) improves the quality factor. The

self-resonance frequency and the inductance, however, do not change. It should also be emphasized that the dynamic range of cascode gyrator-C active inductors is smaller as compared with that of gyrator-C active inductors.

Table 2.2. Comparison of gyrator-C and cascode gyrator-C active inductors.

Parameter	Gyrator-C	Cascode gyrator-C
Zero (ω_z)	$\frac{g_{o1}}{C_{gs2}}$	$\left(\frac{g_{o1}}{C_{gs2}}\right)\frac{1}{g_{m3}r_{o3}}$
Self-resonance freq.(ω_o)	$\sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}}$	$\sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}}$
Inductance (L)	$\frac{C_{gs2}}{g_{m1}g_{m2}}$	$\frac{C_{gs2}}{g_{m1}g_{m2}}$
Series resistance (R_s)	$\frac{g_{o1}}{g_{m1}g_{m2}}$	$\frac{g_{o1}}{g_{m1}g_{m2}}\left(\frac{1}{g_{m3}r_{o3}}\right)$
Parallel resistance (R_p)	$\frac{1}{g_{m1}}$	$\frac{1}{g_{o2}}$
Quality factor (Q)	$\frac{\omega L}{R_s} = \omega C_{gs2}g_{o1}$	$\frac{\omega L}{R_s} = \omega C_{gs2}g_{o1}(g_{m3}r_{o3})$

The performance can be further improved using regulated cascode and multi-regulated cascode to further reduce R_s, as shown in Fig.2.33. Table 2.3 tabulates the parameters of gyrator-C active inductors including cascodes and regulated cascodes.

Table 2.3. Parameters of gyrator-C active inductors.

Active inductor	G_{o1}	C_1	G_{o2}	C_2
Basic	g_{o1}	C_{gs2}	g_{o2}	C_{gs1}
Cascode	$1/[g_{o1}(r_{o3}g_{m3})]$	C_{gs2}	g_{o2}	C_{gs1}
Regulated cascode	$1/[g_{o1}(r_{o3}g_{m3})(r_{o4}g_{m4})]$	C_{gs2}	g_{o2}	C_{gs1}
Multi-regulated cascode	$1/[g_{o1}(r_{o3}g_{m3})(r_{o4}g_{m4})(r_{o5}g_{m5})]$	C_{gs2}	g_{o2}	C_{gs1}

Q-Enhanced Gyrator-C Active Inductors

To improve the quality factor of active inductors, R_p should be maximized and R_s should be minimized. Cascode implemented in the positive transconductors improves the quality factor by lowering R_s from $R_s = \frac{g_{o1}}{g_{m1}g_{m2}}$ to $R_s = \frac{g_{o1}}{g_{m1}g_{m2}}\left(\frac{1}{g_{m3}r_{o3}}\right)$ and increasing R_p from $R_p = \frac{1}{g_{m1}}$ to $R_p = \frac{1}{g_{o2}}$. Because the output impedance of deep sub-micron MOS-

FETs is rather small [27], the negative impact of $R_p = \frac{1}{g_{o2}}$ on the quality factor remains significant. The effect of R_p, however, can be offset by connecting a negative resistor of resistance $\hat{R}_p = -R_p$ in parallel with R_p such that the overall parallel resistance is infinite. Negative resistors can be realized using transconductors with positive feedback, as shown in Fig.2.34 [78, 79]. For the negative resistor shown in Fig.2.34(b), the impedance at low frequencies is given by $Z \approx -\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right)$. To maximize the frequency range over which a constant negative resistance exists, the transconductors synthesizing negative resistors should be configured as simple as possible.

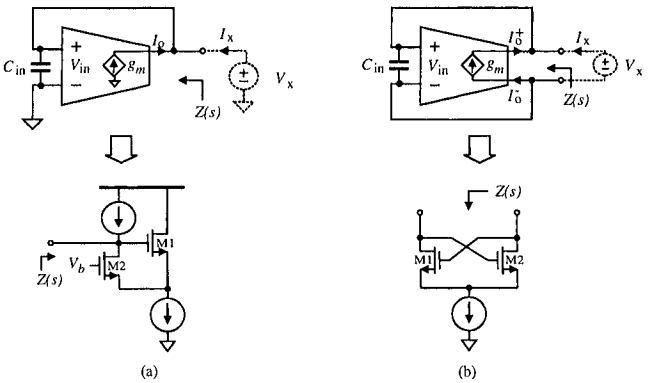

Figure 2.34. Transconductors-based negative impedance networks. (a) Single-ended; (b) Fully differential.

Floating Gyrator-C Active Inductors

For applications such as image rejection filters for RF front-ends, floating inductors are required. Floating active inductors can be realized using differential gyrators, as shown in Fig.2.35. Fig.2.36 give the implementation of floating active inductors reported in [58, 76, 67]

Self-Biased Active Inductors

The self-biased active inductors shown in Fig.2.37 employ only a MOSFET and a resistor without a closed loop [80, 61, 68, 69]. No explicit bias is required. The impedance of the active inductor is given by

$$Z(s) \approx \left(\frac{1}{RC_{gs}C_{gd}}\right) \frac{sRC_{gd}+1}{s^2 + s\frac{g_m}{C_{gs}} + \frac{g_m}{RC_{gs}C_{gd}}}, \tag{2.47}$$

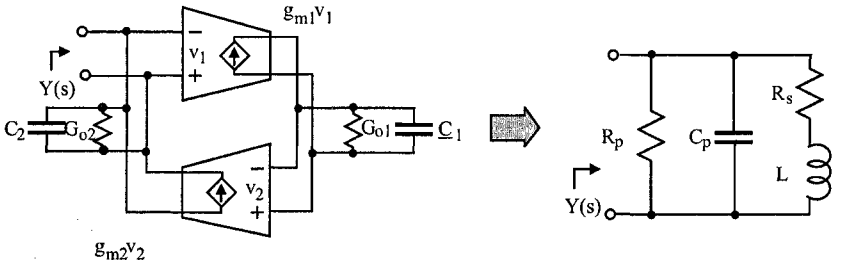

Figure 2.35. Floating gyrator-C active inductors.

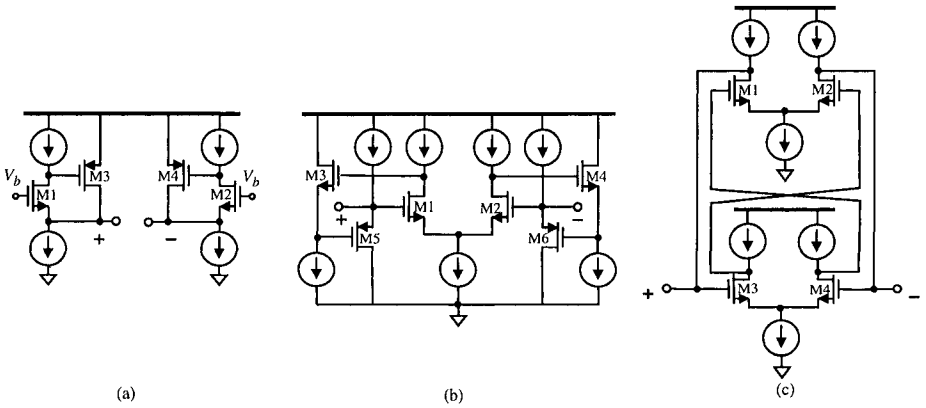

Figure 2.36. Typical configuration of floating gyrator-C active inductors.

where $g_m \gg g_o$ and $C_{gs} \gg C_{gd}$ were used to simplify analysis. The equivalent inductance L and series resistance R_s of the self-biased active inductor are given by

$$\begin{aligned} R_s(\omega) &= \frac{g_m+\omega^2 C_{gs}^2 R}{g_m^2+\omega^2 C_{gs}^2}, \\ L(\omega) &= \frac{C_{gs}(g_m R-1)}{g_m^2+\omega^2 C_{gs}^2}. \end{aligned} \tag{2.48}$$

We have neglected C_{gd}, C_{sb}, C_{sb}, and other high-order effects in derivation of (2.48). Observe that $g_m R > 1$ is required to ensure that the network is inductive. The self-resonant frequency and the frequency of the zero are given by $\omega_o = \sqrt{\frac{g_m}{RC_{gs}C_{gd}}}$ and $\omega_z = \frac{1}{RC_{gd}}$. It exhibits an inductive characteristic when $\omega_z < \omega < \omega_o$. The dependence of the impedance of the active inductor on R and the width of the transistor is shown in Figs.2.38 and Fig.2.39, respectively. It is observed that an

increase in R lowers both ω_z and ω_o. Increasing the width of the transistor lowers ω_o because $\frac{g_m}{C_{gs}}$ is nearly independent of the width of the transistor. Also observed is that the inductance of the active inductor is more sensitive to R. A major drawback of self-biased active inductors is the loss of the voltage headroom of V_T.

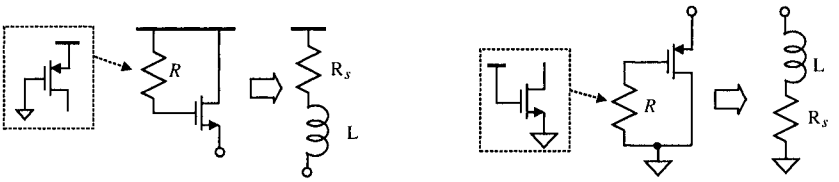

Figure 2.37. Self-biased active inductors.

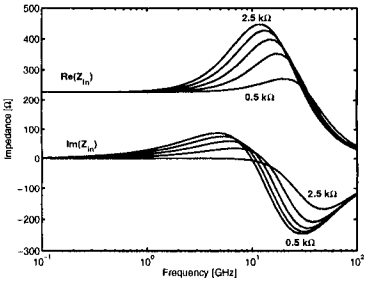

Figure 2.38. Dependence of $Z(s)$ of self-biased active inductor on R. R is varied from 0.5 kΩ to 2.5 kΩ with step 0.5 kΩ, $W = 10\mu$m.

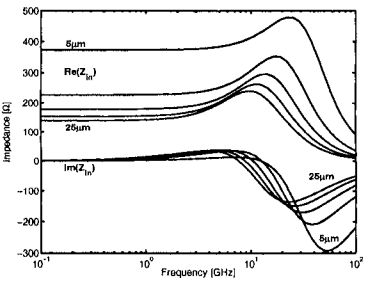

Figure 2.39. Dependence of $Z(s)$ of self-biased active inductor on W. W is varied from 5μm to 25μm with step 5μm, $R = 1k\Omega$.

2.8.2 Noise of Active Inductors

The noise of an active inductor can be represented by a noise-voltage generator denoted by $\overline{v_n^2}$ and a noise-current generator denoted by $\overline{i_n^2}$ at the input port of the active inductor. Because active inductors are 1-port networks, the conventional approaches for deriving the input-referred noise voltage and noise current generators of 2-port networks given in [81, 82] are not applicable.

Noise of Transconductors

To analyze the noise of gyrator-C active inductors, the power of the input-referred noise-voltage generator and that of the noise-current generator of both positive and negative transconductors, as shown in

Fig.2.40, are needed. They can be derived using the conventional approach for 2-port networks [50] and are tabulated in Table 2.4. Note that $\overline{i_{nD}^2} = 4kT(\gamma + R_g g_m)g_m \Delta f$ is the noise of MOSFET consisting of both the thermal noise of the channel resistance and that of the gate series resistance.

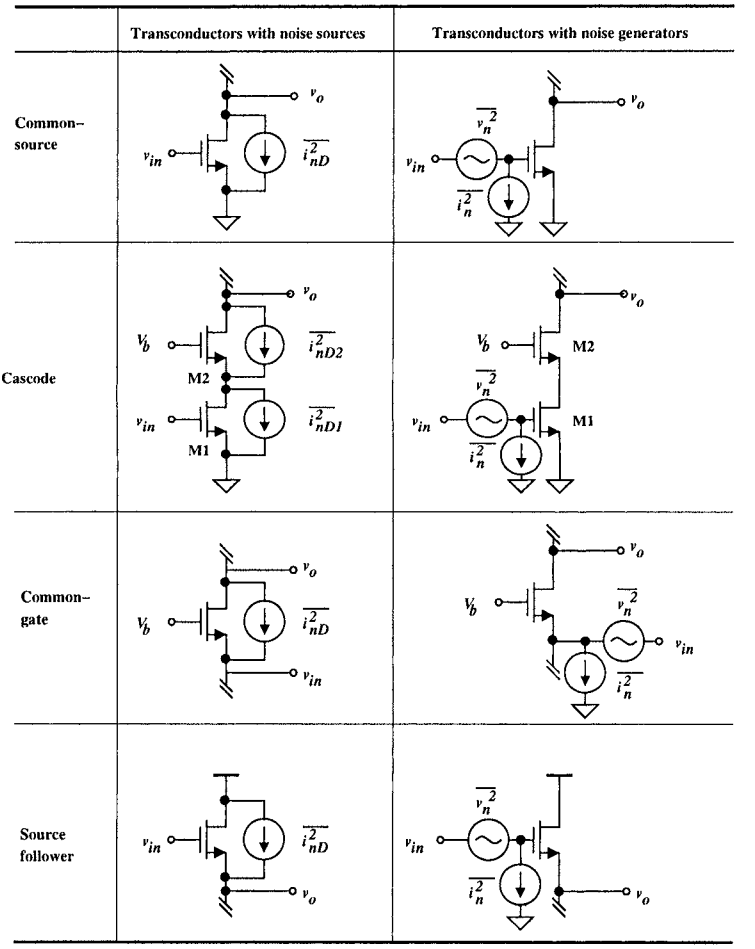

Figure 2.40. Input-referred noise generators of transconductors.

Noise of Gyrator-C Active Inductors

Consider the active inductor of Fig.2.41(a). v_{n1} and v_{n2} are the noise-voltage generators of the transconductors 1 and 2, respectively.

Table 2.4. Input-referred noise generators of transconductors

Transconductor	$\overline{v_n^2}$	$\overline{i_n^2}$
Common-source	$\overline{v_n^2} = \frac{\overline{i_{nD}^2}}{g_m^2}$	$\overline{i_n^2} = 0$
Cascode	$\overline{v_n^2} = \frac{\overline{i_{nD1}^2}}{g_{m1}^2} + \frac{\overline{i_{nD2}^2}}{(g_{m1}r_{o1}g_{m2})^2}$	$\overline{i_n^2} = 0$
Common-gate	$\overline{v_n^2} = \frac{\overline{i_{nD}^2}}{g_m^2}$	$\overline{i_n^2} = 0$
Source-follower	$\overline{v_n^2} = \frac{\overline{i_{nD}^2}}{g_m^2}$	$\overline{i_n^2} = 0$

In Fig.2.41(b), $\overline{v_n^2}$ and $\overline{i_n^2}$, the noise-voltage and noise-current generators, are used to represent the total noise of the inductor. It is trivial to show from Fig.2.41(a) that

$$\overline{v_1^2} = \overline{\left(v_{n1} + Y_1 \frac{g_{m2}v_{n2} + Y_2 v_{n1}}{Y_2 + g_{m1}g_{m2}} \right)^2}. \tag{2.49}$$

For Fig.2.41(b), we have

$$\overline{v_1^2} = \overline{\left(v_n + \frac{Y_1}{Y_1Y_2 + g_{m1}g_{m2}} i_n \right)^2}. \tag{2.50}$$

To ensure that the right hand-side of (2.49) and that of (2.50) are the same, we impose $v_n = v_{n1}$ and $i_n = Y_2 v_{n1} + g_{m2}v_{n2}$. Because $Z_{in}(s) = \frac{Y_1}{Y_1Y_2 + g_{m1}g_{m2}}$, we arrive at $V_n = V_{n1} + Z_{in}I_n$. Further $Y_1 = g_{o1} + sC_1$ and $Y_2 = g_{o2} + sC_2$, we have

$$\begin{aligned} v_n &= v_{n1}, \\ i_n &= (g_{o2} + sC_2)v_{n1} + g_{m2}v_{n2}. \end{aligned} \tag{2.51}$$

Noise of Q-Enhanced Gyrator-C Active Inductors

Consider the negative resistor of Fig.2.42 where $\overline{\hat{v}^2}_n$ is the noise-voltage generator of the transconductor. Note that $\overline{\hat{i}^2}_n = 0$ for ideal transconductors. The output noise power is given by $\overline{v_1^2} = \overline{\hat{v}_n^2}$. Because negative resistors are usually connected in parallel with the inductor

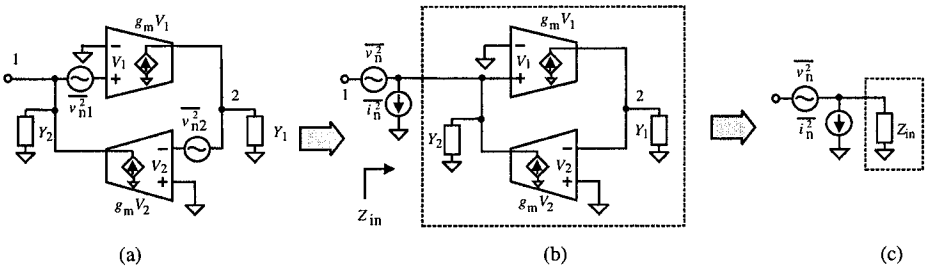

Figure 2.41. (a) Grounded gyrator-C active inductors with noise sources; (b,c) Grounded gyrator-C active inductors with input-referred noise-voltage and noise-current generators.

whose Q is to be enhanced, we use a noise-current generator $\overline{i_{nr}^2}$ only to represent the overall noise of the negative resistor with $\overline{v_1^2} = \frac{\overline{i_{nr}^2}}{g_m^2}$. This leads to $\overline{i_{nr}^2} = g_m^2 \overline{\hat{v}_n^2}$. Consider Fig.2.42(b). It is trivial to show that at low frequencies

$$\overline{(v_1 - v_2)^2} = \frac{\overline{i_{n1}^2}}{g_{m1}^2} + \frac{\overline{i_{n2}^2}}{g_{m2}^2}. \tag{2.52}$$

Use the noise-current generator $\overline{i_{nr}^2}$ to represent the overall noise of the negative resistor. It can be shown that

$$\overline{(v_1 - v_2)^2} = \left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right)^2 \overline{i_{nr}^2}. \tag{2.53}$$

Equating (2.52) and (2.53) yields

$$\overline{i_{nr}^2} = \frac{1}{(g_{m1} + g_{m2})^2}\left[g_{m2}^2 \overline{i_{n1}^2} + g_{m1}^2 \overline{i_{n2}^2}\right] \tag{2.54}$$

The noise-voltage and noise-current generator of Q-enhanced active inductors, denoted by $\overline{v_{n,Q}^2}$ and $\overline{i_{n,Q}^2}$, respectively, can be obtained from Fig.2.43 directly with $\overline{v_{n,Q}^2} = \overline{v_n^2}$ and $\overline{i_{n,Q}^2} = \overline{i_n^2} + \overline{i_{nr}^2}$. Q-enhanced active inductors exhibit a high level of noise power. Also, because the total capacitance of the Q-enhanced active inductor is obtained from $C_{p,Q} = C_p + C_{np}$, where C_{np} is the input capacitance of the negative resistor, we have the self-resonant frequency of the Q-enhanced active inductor $\omega_{o,Q} = \omega_o \sqrt{\frac{C_p}{C_p + C_p}}$.

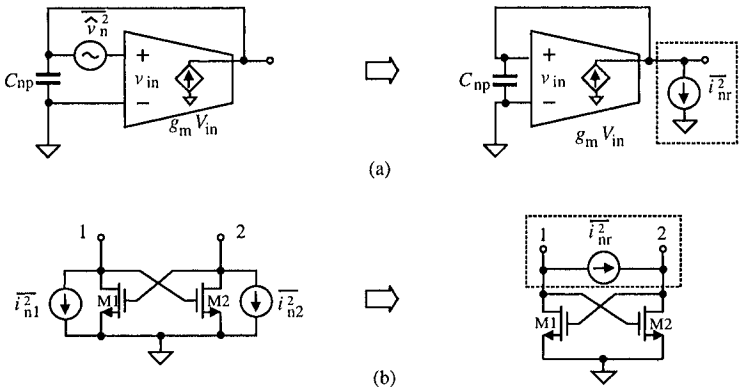

Figure 2.42. (a) Noise of single-ended negative resistors; (b) Noise of floating negative resistors.

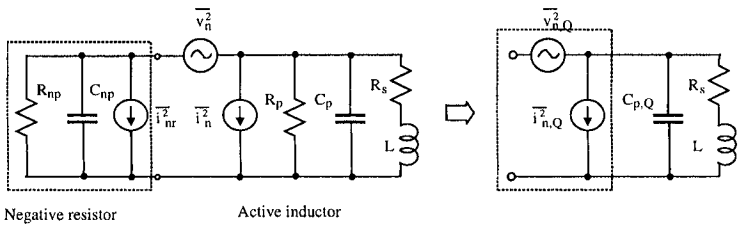

Figure 2.43. Noise equivalent circuit of Q-enhanced active inductors.

2.8.3 Dynamic Range

The dynamic range of an active inductor is defined as the ratio of the maximum allowable signal at the terminals of the inductor to the root-mean-square (RMS) value of the noise power of the active inductor at the same nodes over the frequency range of the active inductor. The maximum signal V_{max} is usually the amplitude of the voltage across the inductor when 1% of total harmonic distortion is observed [83]. For communication circuits, the 3rd-order inter-modulation is usually used to determine V_{max} [84]. The amplitude of the signal at which the distortion level equals to the noise level is also used for V_{max} [85].

2.9 Summary

Design techniques for low-voltage CMOS current-mode circuits have been examined in detail. We have shown that as compared with class A current amplifiers, class AB current amplifiers offer a large signal swing at the expense of a high supply voltage. Cascode and regulated

cascode current amplifiers offer a larger output impedance, however, at the cost of a high supply voltage. Their frequency characteristics are comparable to those of basic current amplifiers. Pseudo-cascode current amplifiers have the same output impedance as that of basic cascode current amplifiers but require a lower supply voltage. Low-voltage cascode current amplifiers offer comparable performance as that of basic cascode current amplifiers, however, at a reduced supply voltage. The use of active feedback effectively lowers the input impedance of current amplifiers. Bootstrapping is an effective means to achieve both a low input impedance and a large output impedance.

Resistor series peaking and inductor series peaking techniques are effective means to increase the bandwidth of CMOS current-mode circuits. The former improves bandwidth by introducing a zero whereas the latter adds a pole. Both resistor / inductor series peaking and current feedback can be employed simultaneously to further improve bandwidth. This approach also reduces the value of the peaking resistors / inductors.

Two main drawbacks of current amplifiers are mismatch-induced output offset currents and high level of static power consumption. The biasing-dependent output offset current can be minimized effectively using the balancing network technique. The level of static power consumption can be reduced by using the current-branching technique. The reduction in the size of the transistors from current-branching also improves bandwidth.

The large and tunable inductance, virtually no chip area requirement, and fully compatible with standard CMOS technologies of CMOS active inductors make them an effective means for performance enhancement of CMOS current-mode circuits. The self-resonant frequency of gyrator-C active inductors is set by the cut-off frequency of the transconductors of the gyrator pairs. The lower bound of the frequency range over which gyrator-C is inductive is set by the output impedance of the transconductors. Cascode gyrator-C inductors lower the lower bound of the frequency without affecting both the effective inductance and self-resonant frequency. The quality factor of active inductors is mainly set by the parasitic series resistance of the inductors and can be improved by increasing the output impedance or the transconductance of the transconductors. The noise of gyrator-C active inductors is proportional to the noise of the transconductors. To minimize the noise and maximize the useful frequency range, the transconductors should be configured as simple as possible.