Chapter 2

Fabrication Processes for Integrated Circuits

Integrated Circuit designs will be realised in one of a number of possible fabrication processes. The circuit fabricated on a die will then be packaged within a suitable protective housing. The particular fabrication process to use will be dependent on a number of issues including cost, availability, experience in the use of, and circuit component capabilities.

2.1 Introduction

A number of fabrication processes exist for realising microelectronic circuit designs. In the main, CMOS (Complementary Metal Oxide Semiconductor) technology is dominant, with a number of key advantages over the alternative processes. However, the available fabrication processes are classified as:

- Bipolar
- CMOS Complementary Metal Oxide Semiconductor
- BiCMOS Bipolar and CMOS
- SiGe BiCMOS Silicon germanium BiCMOS
- GaAs Gallium arsenide
- Memory

The above processes will be reviewed, with detail given to CMOS technology. These fabrication processes will be required to support the design and realisation of specific circuit components, the availability of components being dependent on the particular process. In the main, the following circuit components will be required:

- Transistor
- Diode

- Resistor
- Capacitor
- Inductor

In digital circuits, the transistor is the key circuit component used and digital processes will be optimised to support this. In analogue and mixed-signal processes, the use of high quality resistors, capacitors and potentially inductors, will be required in addition to the transistor. The basic structure of the IC die is shown in Fig. 2.1. Here, the circuit is fabricated within the die and this is mounted in a suitable package.

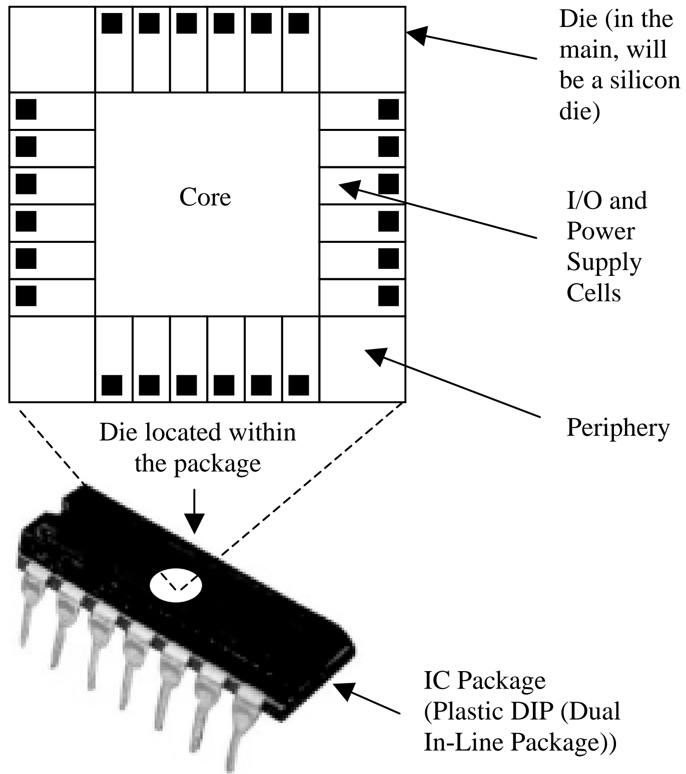


Fig. 2.1. Structure of the IC

The (silicon) die will be square or rectangular in shape and will be fabricated on a wafer. The die will have two identifiable areas, the periphery and the core:

- The core contains the bulk of the circuitry.
- The periphery will contain Input/Output cells and Power Supply cells. These cells are physically much larger than the core cells and will be required to bond the die to the package, as well as providing Electrical Overstress (EOS) protection.

The die is mechanically secured to the package and electrically bonded to the package pins. Electrical, mechanical and thermal considerations must be taken into account in the choice of the package used.

2.2 Technology Nodes

Driven by the need for higher levels of integration and higher operating frequencies for digital systems, the move is to reduce the circuit component geometries. This allows for more components per mm^2 of die area and a reduction in the interconnect lengths between components. There are two main figures given to represent the level of integration:

- Minimum transistor gate length
- Technology node

The **minimum transistor gate length** defines the smallest transistor gate length that can be designed (this is the **printed gate length**) by the designer. Once fabricated, this will actually be smaller due to processing issues (this is the **physical gate length**). For example, a 0.18 µm CMOS process would define a minimum printed MOSFET transistor gate length of 0.18 µm. The minimum gate length figure has been linked to microprocessor unit (MPU) and ASIC (Application Specific Integrated Circuit) devices.

The **technology node** is also used as a metric, and has been historically linked to the introduction of new generations of DRAM (Dynamic Random Access Memory). The figure quoted is the DRAM lithography half-pitch. In the International Technology Roadmap for Semiconductors (ITRS) 2003 edition [1-4], the predicted gate lengths and DRAM ½ pitch dimensions are linked. The roadmap is separated into near years (2003-2009) and far years (2010-2018). Table 2.1 provides a snapshot of the ITRS technology nodes at three points in time and an example of the Austria Mikro Systems (AMS) [20] process roadmap.

Table 2.1. Example available roadmaps and fabrication processes

Source	Year		
	2005	2010	2015
ITRS Roadmap Technology Node (DRAM ½ pitch (nm))	80	45	25
ITRS Roadmap Technology Node (printed gate length (nm))	45	25	14

	Roadmap Fabrication Processes		
Austria Mikro Systems (AMS) (roadmap 2006 onwards – for the 0.18 µm process) [20]	Mixed-Signal/RF CMOS	SiGe BiCMOS	High Voltage CMOS
	High Speed Opto-CMOS	One Time Programmable / Non-Volatile Memory	

2.3 Wafer Size

The wafer size (wafer diameter) has been increasing over recent years so that now the wafer diameters have progressed from 4” through 6” and 8” to the current 12” (300 mm) diameter. It is not predicted that the wafer diameter will increase beyond 300 mm for the foreseeable future due to cost issues.

The circuit dies are initially fabricated on the wafer, these being circular slices of semiconductor material (*e.g.* silicon). The wafer contains multiple copies of a single die, or may contain multiple copies of several die designs, along with process monitor die, see Fig. 2.2. The number and types of monitor die design depend on the maturity of the process – a new fabrication process will have different process monitoring requirements than a mature fabrication process.

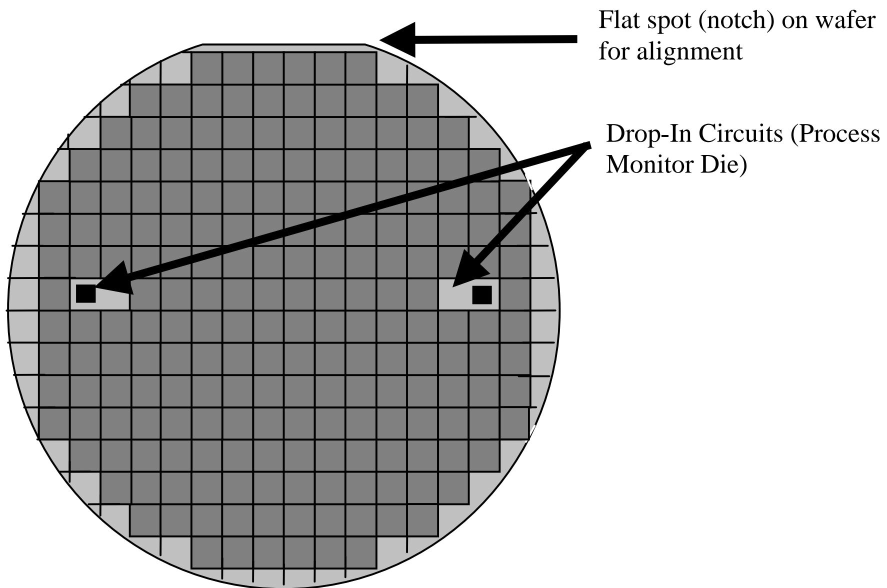


Fig. 2.2. Silicon wafer

Where several die designs are placed on the silicon wafer, this is referred to as a **Multi-Project Wafer** (MPW). These contain multiple “project” designs and would be used for design prototyping in that only a small number of dies are typically required (much less than a wafer can readily contain). The wafer fabrication costs can be spread across multiple projects and so reduce the design prototyping costs. With the introduction of 300 mm wafers, the ability for each wafer to contain more copies of a die can aid in the reduction of the fabrication costs of the die. However, the necessary fabrication equipment purchase and operational costs for the lower process geometries are much higher than those for the coarser process geometries using smaller diameter wafers. The cost implications and potential cost benefits need careful consideration.

2.4 Bipolar Technology

Within the bipolar process [5, 6], the fabrication of the bipolar transistor (BJT – Bipolar Junction Transistor) is of primary concern, although a fabrication process may also support other forms of component (in particular the inclusion of resistors and capacitors). The bipolar process was the only available technology available in the early years of IC fabrication and today, bipolar transistors are used for their advantages in high-speed operation (*e.g.* communication systems) and high-current drive capability for power applications (*e.g.* automotive). However, they do not allow for the high levels of integration and low-power operation that can be achieved with CMOS (see next section).

The bipolar transistor is based around a sandwich of n and p-type silicon, see Fig. 2.3.

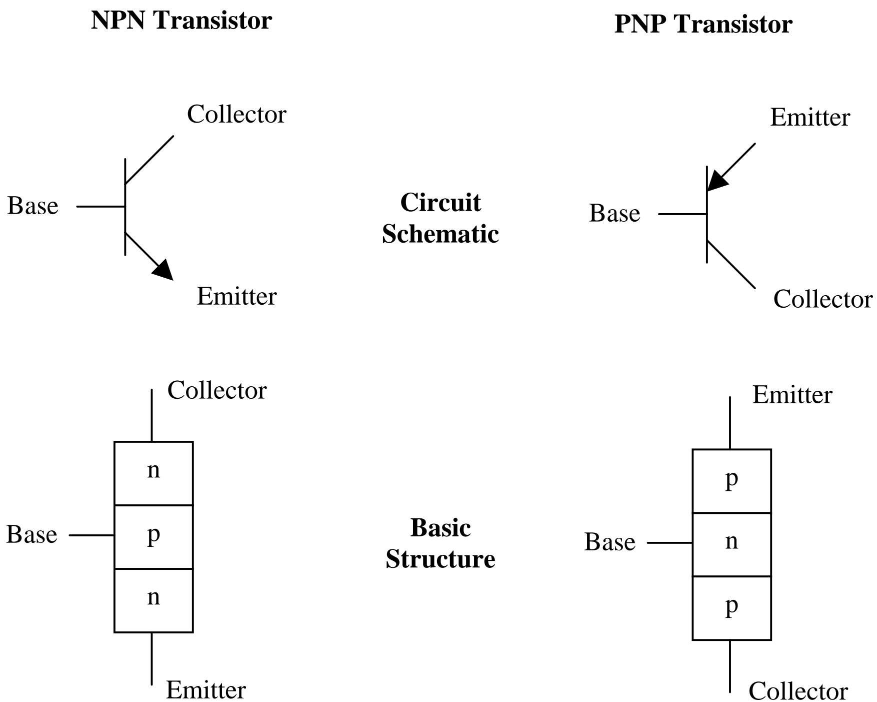


Fig. 2.3. Bipolar transistor forms

The basic operation, with reference to the NPN transistor, is that a current flowing into the base of the transistor (and exiting out of the emitter) allows for a larger collector current to flow from the collector through to the emitter. This current gain can be used to implement analogue (*e.g.* amplification) and digital (*e.g.* digital

logic) functions. In the diagrams shown in Fig. 2.3, a 4th connection (substrate) connection has been omitted, although this would need to be accounted for in an IC design.

2.5 Complementary Metal Oxide Semiconductor (CMOS) Technology

Following on from the early days of the bipolar fabrication process, the Complementary Metal Oxide Semiconductor (CMOS) [7-9] fabrication process has been the mainstay of the microelectronics industry since the early 1970s. In this, the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is of primary concern, although a fabrication process may also support other forms of component (in particular the inclusion of resistors and capacitors). Additionally, a CMOS fabrication process can also include the ability to fabricate bipolar transistors, although these tend to be of low performance when compared to the device performance available in a bipolar fabrication process. Today, CMOS is used for many circuit applications from digital processors through to data converters and analogue amplifiers. CMOS is based on two types of MOS transistor – the nMOS transistor and the pMOS transistor. This is a follow-on from the earlier nMOS fabrication process which allowed for the fabrication of nMOS devices. The MOS transistor is based around an insulated gate which controls the flow of current by varying the voltage on the insulated gate, see Fig. 2.4.

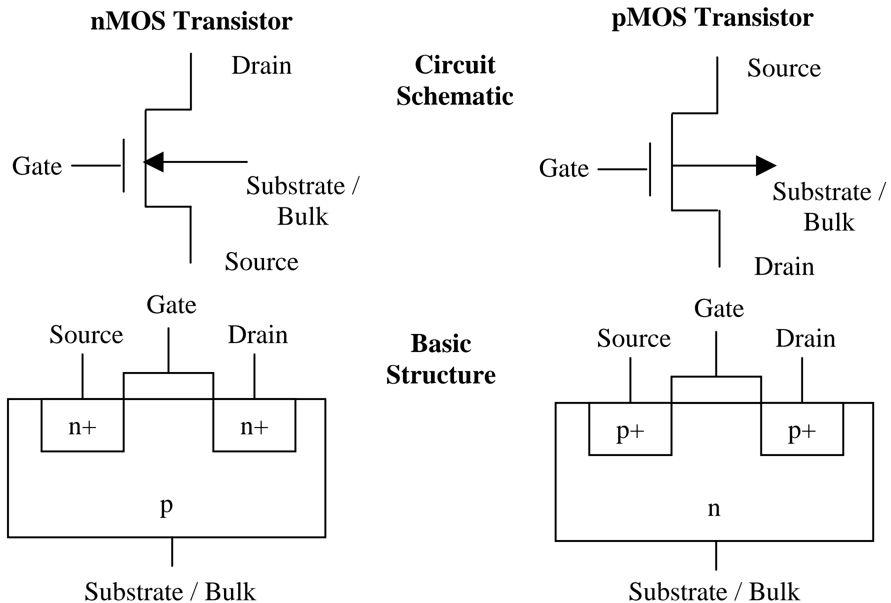


Fig. 2.4. MOS transistor forms

Here, the transistor has four connections (gate, drain, source and substrate (or bulk)). With reference to the nMOS transistor, a positive voltage between the gate and source allows for a current to flow between the drain and source. By varying the gate-source voltage, the drain current will vary. This operation can be used to implement analogue (*e.g.* amplification) and digital (*e.g.* digital logic) functions.

A 3D view of the nMOS transistor is shown in Fig. 2.5.

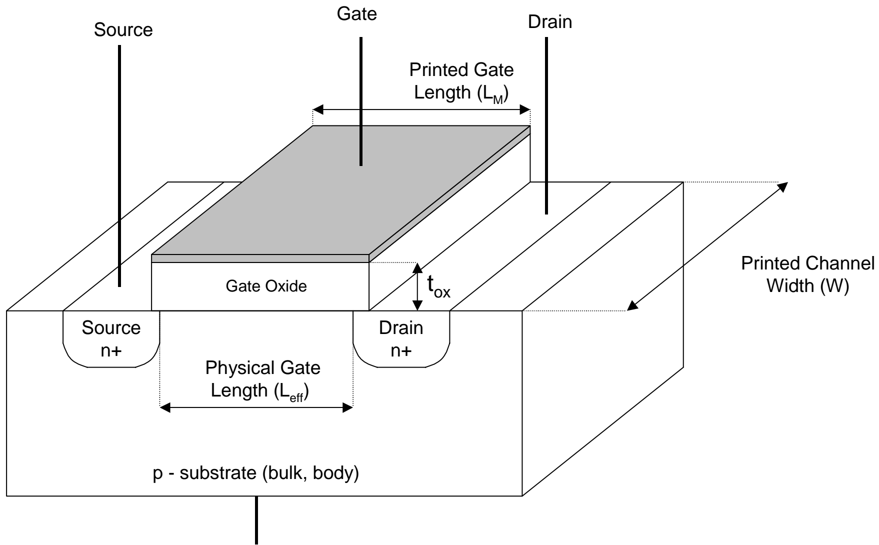


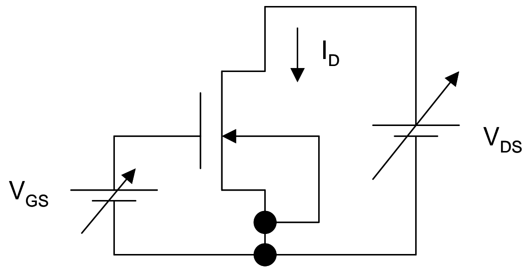
Fig. 2.5. 3D view of the nMOS transistor (simplified)

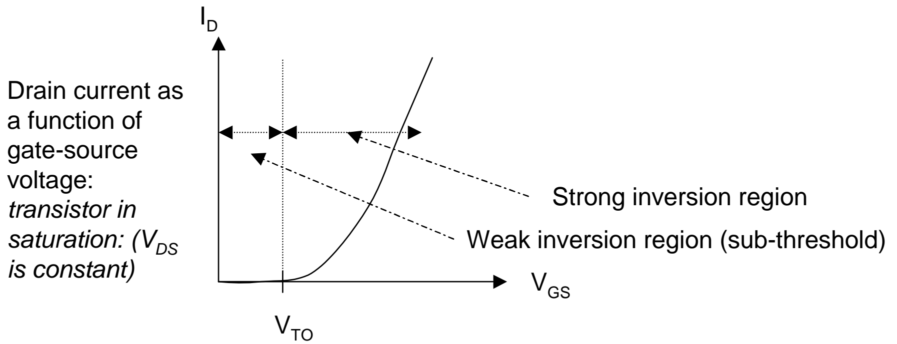
The printed gate length (L_M), the physical gate length (L_{EFF} – effective gate length) and the insulating gate oxide thickness (t_{ox}) are shown.

The operation of the MOSFET is considered with respect to:

- Gate-source voltage (V_{GS}) vs drain current (I_D).
- Drain-source voltage (V_{DS}) vs drain current (I_D) for various gate-source voltage values.

The transistor can operate in both a linear region (the transistor acts as a voltage controlled resistor) and a saturation region (the transistor acts as a voltage controlled current source). Figure 2.6 shows the basic relationship plots for the nMOS transistor. When the gate-source voltage is below a threshold voltage (V_{TO}), the drain current is, to a first approximation, zero. It is however small but finite – this is the sub-threshold current. It is this small sub-threshold current that gives CMOS its low-power operation capability and the effect is used in I_{DDQ} testing for digital logic. However, with the smaller transistor gate lengths found in deep submicron (DSM) processes, this sub-threshold current is significantly larger.





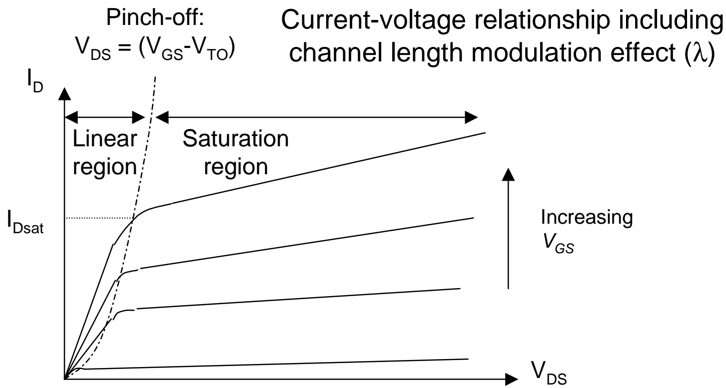
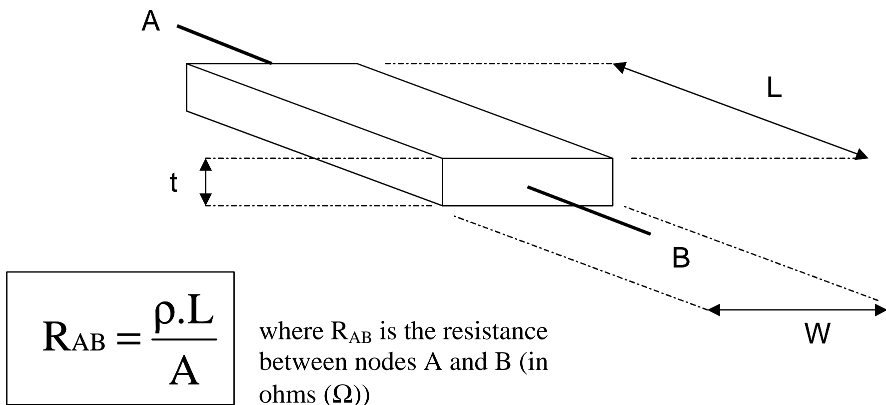


Fig. 2.6. V_{GS} / V_{DS} vs I_D plots

In addition to the MOSFET, the CMOS fabrication process will also be capable of implementing passive components (resistors, capacitors and, to a very limited extent, inductors), along with a basic bipolar transistor. With the resistor and capacitor, there are a number of variants on the basic R and C, see Figs. 2.7 and 2.8. In Fig. 2.7, a layer within the CMOS process will have a certain resistivity (ρ). By defining a suitable shape of material (and assuming that the thickness of the layer will remain constant), a resistor can be fabricated. Resistors are however physically large (when compared to transistors) and it is difficult to fabricate accurate values.



Where A is the cross-sectional area (W.t)

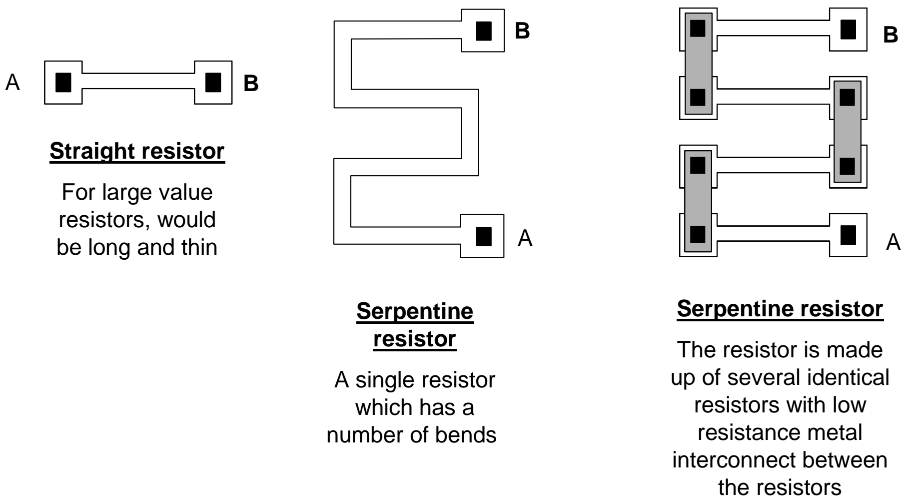


Fig. 2.7. Resistor structures in CMOS

In Fig. 2.8, the capacitor is fabricated with two conductors separated by an insulator (dielectric). This forms a capacitor structure. A range of capacitor structures can be formed in the CMOS process.

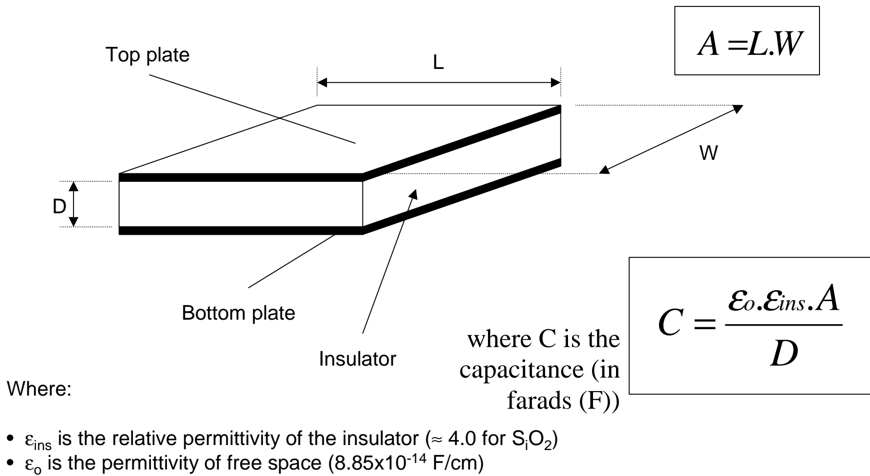


Fig. 2.8. Capacitor structure in CMOS

The layout will be designed according to a set of design rules for the particular fabrication process. These design rules will have been generated to allow for a high overall yield (working circuits after fabrication) and reliability of the circuits, whilst using the smallest possible area. For a design to be accepted for fabrication, the layout must conform to the layout design rules (except in special agreed situations). The design layout, during and after creation, would be checked by the designer by running a **DRC** (Design Rules Checking) procedure. This would "access" the layout design rules and check that the layout does not violate any of these. The designer would need to ensure that there were no **DRC errors** (an error being a violation of a layout design rule).

Layout design rules are usually described in one of two forms:

- **Micron Rules** — The layout constraints are defined in terms of absolute dimensions (μm).
- **Lambda (λ) Rules** — The layout constraints are defined in terms of a single parameter (λ). This λ parameter has an absolute dimension (μm).

Lambda-based rules allow for linear, proportional scaling of the geometries and were originally devised to simplify industry-based micron rules, also allowing for scaling of various processes.

For fabrication, the layout will be exported from the CAD (Computer Aided Design) tool to a file that will describe the circuit layout in a suitable format. The two file formats used are:

- GDSII Stream File Format
- CIF Caltech Intermediate Format

CIF is a low-level graphics language for defining layout geometries. The CIF file consists of a number of statements (and where appropriate, comments). This is a machine-independent ASCII text file. Consider the CMOS inverter shown in Fig. 2.9. Here, the design is a static CMOS logic inverter shown as a schematic (left) and a layout (right).

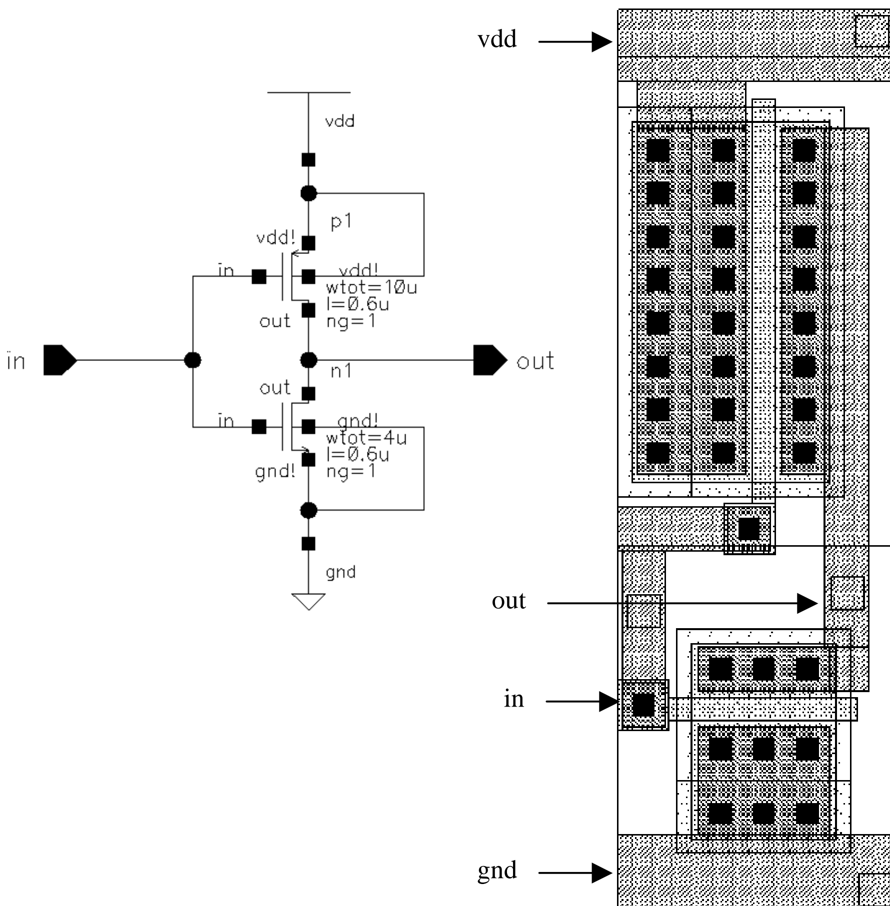


Fig. 2.9. Schematic diagram and layout for a CMOS inverter

An example of a CIF file describing this inverter layout is shown in Fig. 2.10. This file contains information on the geometries on each layer that are used to create the inverter design (the transistors and metal interconnect). All dimensions are in centimicrons.

```
(CIF file for Inverter cell);

DS 1 1 1;

9 Inverter;

L NWELL;
B 760 1360 380,1680;

L PPLUS;
B 480 200 400,250;
B 420 1080 410,1680;

L DIFF;
B 400 540 400,460;
B 540 1000 310,1680;

L NPLUS;
B 480 420 400,560;
B 200 1080 100,1680;

L POLY1;
B 520 60 400,550;B 140 140 70,560;
B 140 140 360,1050;B 60 1120 400,1680;

L CONTACT;
B 60 60 280,260;B 60 60 400,260;
B 60 60 520,260;B 60 60 280,440;
B 60 60 400,440;B 60 60 520,440;
B 60 60 280,660;B 60 60 400,660;
B 60 60 520,660;B 60 60 110,2100;
B 60 60 110,1980;B 60 60 110,1860;
B 60 60 110,1740;B 60 60 110,1620;
B 60 60 110,1500;B 60 60 110,1380;
B 60 60 110,1260;B 60 60 290,2100;
B 60 60 290,1980;B 60 60 290,1860;
B 60 60 290,1740;B 60 60 290,1620;
B 60 60 290,1500;B 60 60 290,1380;
B 60 60 290,1260;B 60 60 510,2100;
B 60 60 510,1980;B 60 60 510,1860;
B 60 60 510,1740;B 60 60 510,1620;
B 60 60 510,1500;B 60 60 510,1380;
B 60 60 510,1260;B 60 60 360,1050;
B 60 60 70,560;

L METAL1;
B 360 120 400,660;B 120 120 70,560;
B 120 120 360,1050;B 120 960 510,1680;
B 300 960 200,1680;B 300 130 200,2225;
B 760 200 380,2390;B 110 120 635,660;
B 120 1440 630,1440;B 120 370 70,805;
B 360 300 400,350;B 300 120 150,1050;
B 760 200 380,100;

DF;
C 1;
E
```

Fig. 2.10. Example CIF file for a CMOS inverter

2.6 BiCMOS Technology

By combining the bipolar and CMOS processes, a BiCMOS process is developed. Here, the low-power and high levels of integration of CMOS and the power drive capabilities of bipolar are integrated. This is desirable for applications that require a large amount of digital signal processing (in CMOS) and actuator drive (in bipolar). An example application would be the automotive industry for the intelligent control of actuators such as DC motors. There is a trade-off required in the performance of each type of transistor required.

2.7 SiGe BiCMOS Technology

Silicon-Germanium (SiGe) [10-12] is a technology that combines the integration and cost benefits of silicon with the speed of more expensive technologies such as gallium-arsenide. In this process, germanium is introduced into the base layer of an otherwise all-silicon bipolar transistor. This creates significant improvements in operating frequency, current, noise, and power capabilities of the resulting transistor when compared to an all-silicon bipolar transistor. The result is a SiGe **Heterojunction Bipolar Transistor** (HBT). The application areas are mainly high frequency (GHz) RF (Radio Frequency) communications circuits and systems. Examples include wireless communications and high-speed data converters.

2.8 Gallium Arsenide (GaAs) Technology

Gallium Arsenide (GaAs) was developed and initially used for IC fabrication to overcome the operating frquency limitations with silicon devices in high frequency RF (Radio Frequency) communications systems applications. The GaAs material electron mobility is much higher than that of silicon and it was put forward as a complement to silicon for high-speed circuits and systems. However, the high fabrication costs have limited its uptake and have mainly been superseded by both improvements in silicon processing and the introduction of SiGe processes.

2.9 Memory Processes

Memory processes are optimised for the high device density required for the integration of high capacity memories and low memory access times:

- RAM   SRAM and DRAM

- ROM PROM, EPROM, EEPROM, FLASH

In particular, the process advances are being driven by the DRAM and FLASH memory market areas requiring increasing memory capacity and faster memories (reducing memory access times for both writing data to the memory and reading data from the memory).

2.10 Packaging

At some point, the die will need to be packaged for protection and further use. Unless the bare die is to be directly mounted onto a substrate (MCM, SiP or PCB), it will be packaged in either a Through-Hole or Surface Mount package type. The package material will be either plastic or ceramic. The following lists the package names referring to the main available types:

Through-Hole Device Package Types

CERQUAD Ceramic Quadruple Side

DIP Dual In-line Package:

- **CERDIP** Ceramic DIP
- **HDIP** Hermetic DIP
- **PDIP** Plastic DIP

SIP Single In-line Package

ZIP Dual In-line Zig-Zag Package

PGA Pin Grid Array:

- **CPGA** Ceramic Pin Grid Array
- **PPGA** Plastic Pin Grid Array
- **SPGA** Staggered Pin Grid Array

Surface Mount Device Package Types

BGA Ball Grid Array:

- **CBGA** Ceramic Ball Grid Array
- **FBGA** Fine Pitch Ball Grid Array
- **PBGA** Plastic Ball Grid Array

CQFP Ceramic Quad Flat Pack

LCC Leadless Chip Carrier*:

CLCC	Ceramic Leadless Chip Carrier
PLCC	Plastic Leadless Chip Carrier

LCC Leaded Chip Carrier*:

JLCC	J-Leaded Chip Carrier
CLCC	Ceramic Leaded Chip Carrier
PLCC	Plastic Leaded Chip Carrier

QFP Quad Flat Pack:

CQFP	Ceramic Quad Flat Pack
PQFP	Plastic Quad Flat Pack
QFJ	Quad Flat Pack (J-lead)
TQFP	Thin Quad Flat Pack
VQFB	Very-thin Quad Flat Pack

SOIC Small Outline IC:

CSOIC Ceramic Small Outline Integrated Circuit

SOP Small Outline Package:

PSOP	Plastic Small-Outline Package
QSOP	Quarter Size Outline Package
SOJ	Small Outline (J-lead Package)
SSOP	Shrink Small-Outline Package
TSOP	Thin Small-Outline Package
TSSOP	Thin Shrink Small-Outline Package
TVSOP	Thin Very Small-Outline Package

Note: * - the leaded and leadless chip carriers can be identified by the same acronyms and can be easily confused.

Packages are defined by the following Military Standards:

- **MIL-STD-1835D** Electronic Component Case Outlines.
- **MIL-HDBL-6100** Case details for Discrete Semiconductor Devices.
- **MIL-STD-2073-1D** Packaging of Microcircuits (Military Packaging).
- **MIL-STD-1285D** Marking of Electrical and Electronic Parts.

2.11 Die Bonding

The bonding of the die to the package is primarily required to allow for electrical connections (signal I/O and power) between the package pins and the die core circuitry. Once the die has been secured to the package (allowing for thermal

bonding for heat removal (using materials with similar Thermal Coefficient of Expansion (TCE) and sometimes electrical connection from the back of the die to the package), the die bonding is required. If the materials have different Thermal Coefficients of Expansion, during device heating and cooling under normal and extremes of operation, thermal stresses may be introduced which can lead to problems in the interconnect such as broken joints.

Wire bonding (using fine gold or aluminum wires), Tape Automated Bonding (TAB) or flip-chip solder bonding allow for the electrical connections to be made.

2.12 Multi-Chip Modules

Many packaged devices will contain a single die. However, there are situations where a package will contain multiple dies, *e.g.* where sensors and circuits are to be housed in a single package but cannot be fabricated on a single die. These types of devices are referred to as **Multi-Chip Modules** (MCMs) [13] and were originally referred to as **Hybrid Circuits**. The MCM is a structure consisting of two or more Integrated Circuits (ICs) and passive components on a common circuit base (substrate), and interconnected by conductors fabricated within that base. The ICs may either be packaged dies or bare dies. This addresses a number of issues relating to the physical size reduction problem and the degradation of signals passing through the packaging and interconnect on a PCB. The MCM may provide advantages in certain electronic applications over a conventional PCB implementation. The advantages include:

- Increased system speed
- Reduced overall size
- Ability to handle ICs with a large number of Inputs and Outputs (I/O)
- Increased number of interconnections in a given area
- Reduced number of external connections for a given functionality

In addition, an MCM may contain dies produced with different fabrication processes within a single packaged solution (e.g. mixing low-power CMOS with high-power Bipolar technologies). There are a number of types of MCMs that can be realised:

MCM-D
Modules whose interconnections are formed by thin film deposition of metals on deposited dielectrics. The dielectrics may be polymers or inorganic dielectrics.

MCM-L
Modules using advanced forms of PCB technologies, forming copper conductors on laminate-based dielectrics.

MCM-C
Modules constructed on co-fired ceramic substrates using thick film (screen printing) technologies to form conductor patterns. The term co-fired relates to the fact that the ceramic and conductors are heated in the oven at one time.

MCM-D/C
Deposited dielectric on co-fired ceramic.

MCM-Si
Silicon based substrate similar to conventional silicon ICs.

It is essential to obtain good quality dies that are known to be fully functional. Obtaining a **Known Good Die** (KGD) is a requirement for MCM design. During the production test of an IC, rather than progressing the die into a packaging stage, it may provided as a KGD to the customer. In this case, it may be necessary to undertake a more rigorous test on the die than would have been undertaken if the die was then to be later packaged and re-tested by the producer. With the ability to provide bare silicon dies, then an electronic system may be produced in one of a number of ways – from bare silicon die through to PCB. There are four package levels:

Die level	Bare silicon die.
Single IC level	Packaged silicon die (a single packaged die).
Intermediate level	An intermediate level where silicon dies (die level) and/or packaged dies (single IC level) are placed onto a suitable substrate that may or may not then be further packaged.
PCB level	Printed Circuit Board.

Combining these four levels, four types of packaged electronics can be identified:

Type 1	Packaged silicon die mounted on a PCB.
Type 2	Packaged silicon die mounted on an intermediate substrate that is then mounted onto a PCB.
Type 3	A bare silicon die mounted on an intermediate substrate that is then mounted onto a PCB.
Type 4	A bare die mounted directly onto a PCB.

Figure 2.11 shows the relationship between package levels and the types of packaged electronics. Package types 2 and 3 are commonly referred to as MCMs.

Package Level	Package Type			
	1	2	3	4
Die level	✱	✱	✱	✱
Single IC level	✱	✱		
Intermediate level		✱	✱	
PCB level	✱	✱	✱	✱

Fig. 2.11. Package levels and types

The MCM structure is in-line with the ITRS definition for a **System in Package** (SiP) device. The ITRS definition for the SiP is:

"*any combination of semiconductors, passives, and interconnects integrated into a single package*"

However, SiP designs [14-18] extend the concept of the MCM from devices placed horizontally side-by-side and bonded to a substrate (as in a PCB), to vertically stacked devices with bonding to the substrate. Wire bonding to the substrate is common.

2.13 Foundry Services

A number of companies provide their own foundry services, either for in-house use or as a service to other organisations. Table 2.2 identifies a number of the key foundry services available.

Table 2.2. Foundry services

Foundry	URL
AMI Semiconductor (AMIS)	http://www.amis.com
Austria Mikro Systems (AMS)	http://www.austriamicrosystems.com
Chartered Semiconductor	http://www.charteredsemi.com
International Business Machines (IBM)	http://www.ibm.com
Hewlett Packard (HP)	http://www.hp.com
Intel Corporation	http://www.intel.com
Maxim	http://www.maxim-ic.com
ST Microelectronics	http://www.st.com
Taiwan Semiconductor Manufacturing Company (TSMC)	http://www.tsmc.com
United Microelectronics Corporation (UMC)	http://www.umc.com

In addition, organisations provide access to tools and foundry services for groups of users (e.g. universities). The two key organisations are:

- **Europractice** http://www.europractice.com
- **Mosis** http://www.mosis.org

2.14 Process Variations

Whenever a wafer is fabricated, each wafer will have variations from each other as to the electrical properties of the circuit components fabricated on the wafer. Additionally, each circuit die on the wafer will vary from each other as to the electrical properties of the circuit components fabricated. It is necessary during the fabrication process to ensure that the process remains within a specific tolerance band. Additionally, it is a common approach for the circuit design to be created so that it will operate according to the required specifications over the guaranteed process variations. Circuit simulation, using a range of component models, will be used by the designer in order to verify the circuit operation (through simulation). With the finer process geometries, the spread in the electrical properties of the individual transistors can be significant and cause for concern.

2.15 Electromigration

Electromigration [5, 6, 19] occurs in the interconnect metal due to high current densities. This is a significant problem when the track widths reduce to narrow dimensions. The current density in the interconnect (amps/m^2) flowing through the small cross-section area of metal can be high enough to cause bulk movement of the metal due to the momentum of the current carrying electrons. This can cause the narrowing of the track width and increased current density. The result will be an increase in the electrical resistance of the track and eventual fusing.

2.16 Future Directions

Future advances [1-4] in the processing and packaging are based on the required end user applications. A summary is provided in Table 2.3.

Table 2.3. Future process issues

Technology driver	Description
Faster operating speeds	Higher signal frequencies Driven by communications applications Reduced device geometries (gate length and gate oxide thickness) Moving onto the next technology node to improve performance of components and reduce interconnect delays Lower k (dielectric constant) dielectrics to

	reduce interconnect delay. A move away from silicon dioxide (SiO_2) to insulators with a lower dielectric constant (k) Low resistivity metal for interconnect. Move away from aluminum interconnect to copper New packaging materials Move into the nanotechnology domain
Higher levels of integration (Higher density)	Reduced device geometries (gate length and gate oxide thickness) Higher k dielectrics for DRAM capacitors to reduce capacitor area Thinner dielectrics for memory devices Reduced package dimensions More pins on a package Move into the nanotechnology domain
Lower operating voltages	A need to improve device reliability by reducing electric field strength in dielectrics Aim to lower device power consumption Portable, battery operated circuits
SoC and SiP devices	Multiple dies and passive components within packages Integration of MEMs (Micro-Electromechanical) devices (*e.g.* sensor integration) Process integration – analogue, digital and memory on the same die

2.17 Summary

This chapter has provided an introduction to the basic fabrication processes and packaging requirements for Integrated Circuits. Whenever a circuit design is to be realised, the right fabrication process and packaging technology must be chosen. This will be dependent on a number of requirements including the availability of a fabrication process and the ability for the process to allow for the circuit functionality to be designed at the right cost. CMOS is by far the most prevalent fabrication process in use today, with bipolar, BiCMOS, SiGe BiCMOS and GaAs also utilised. This chapter has introduced the available processes as an overview with references provided for further reading. The purpose of this was to introduce the basic fabrication processes in order to identify a number of the process issues that will relate to test program development.

2.18 References

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Exercises

Question 1

From the device datasheets, identify the following for the current range of microprocessors used in desktop PCs:

- The device type and manufacturer
- Package type and number of pins
- Number of pins dedicated to the following:
  - Power Supply
  - I/O
  - Test
- Power consumption and cooling requirements

Question 2

Repeat Question 1, except now identify the following for the current range of microprocessors used in notebook PCs.

Question 3

Repeat Question 1, except now identify the following for the current range of microprocessors used in Personal Digital Assistants (PDAs).

Question 4

Identify the applications that use bipolar technology. What is the range of signal frequency that they work with?

Question 5

Identify the applications that use CMOS technology. What is the range of signal frequency that they work with?

Question 6

Identify the applications that use BiCMOS technology. What is the range of signal frequency that they work with?

Question 7

Identify the applications that use SiGe technology. What is the range of signal frequency that they work with?

Question 8

Identify the applications that use GaAs technology. What is the range of signal frequency that they work with?